J202H-I

Wi-Fi Single-band 1X1 802.11b/g/n

IoT Module Datasheet

J202H-I Serial

Module Datasheet

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_____ Title

_____ Signature

_____ Date

_____ Fn-Link

Revision History

Version	Date	Revision Content	Draft	Approved
1.0	2021/06/17	Initial release	Tzq	Qjp
2.0	2021/08/10	Update the picture	Tzq	Qjp

CONTENTS

1 Overview

1.1 Introduction

J202H-I is a Wi-Fi + BLE combination module for low power consumption and high performance application development. The wireless subsystem includes 2.4G radio, Wi-Fi 802.11b/ G /n and BLE 5.0 baseband /MAC designs. The microcontroller subsystem contains a low-power 32-bit RISC CPU, cache, and memory. The power source management unit controls the low power mode. In addition, various security features are supported.

Peripheral interfaces include SDIO, SPI, UART, I2C, IR Remote, PWM, ADC, DAC, PIR and GPIO.

1.2 Features

Wi-Fi General

- supports IEEE 802.11b /g/n protocol
- 2.4GHz band 1T1R mode, support 20 MHz, data rate up to 72.2Mbps
- Wi-Fi Security WPS/WEP/WPA/WPA2 Personal/WPA2 Enterprise/WPA3
- Support Station mode, Softap mode, Station + Softap mode, Sniffer mode
- Bluetooth low energy consumption 5.0, Bluetooth Mesh
- Wi-Fi and BLE coexist
- 5.0 support BLE

MCU Features

- 32-bit RISC CPU with FPU
- 1 RTC timer with a maximum counting cycle of 1 year
- DFS from 1MHz to 192MHz
- Support XIP QSPI Flash startup, built-in image decryption unit

Host Interface

- SDIO 2.0 1x
- SPI 1x
- I2C 1x
- UART 3x
- I2S 1x
- PWM 5x
- ADC 5x
- GPIO 13x

Note: Please refer to chapter 4.3 pin function table for detail host interface configures

The general block diagram of the module is shown as below

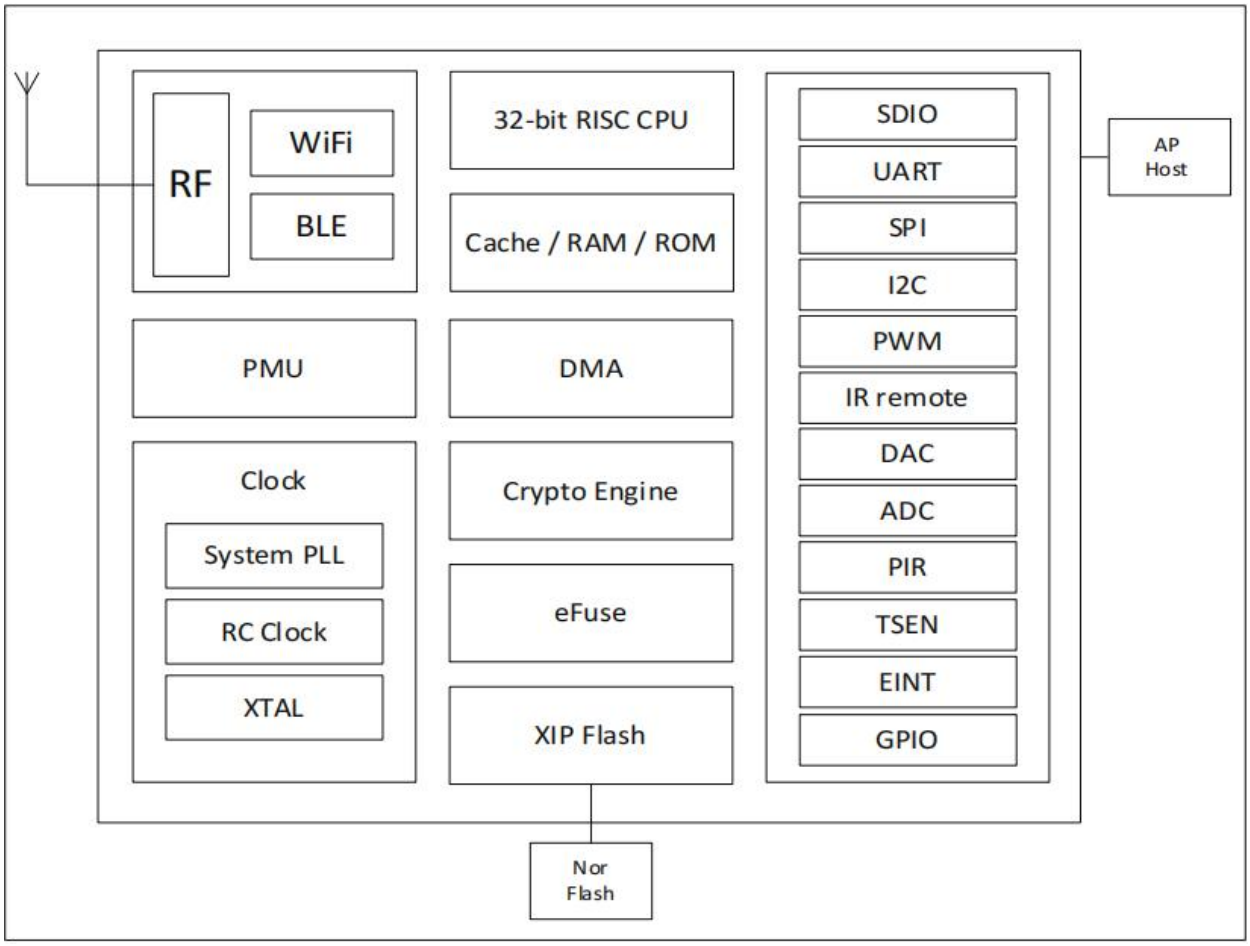


Figure 1-1 Block Diagram

1.3 General Specification

Model Name	J202H-I
Main Chipset	BL602C-20-Q2I(J202H-I)
Host Interface	SDIO, SPI, I2C, UART, I2S, PWM, ADC, GPIO
Wi-Fi Standards	802.11b/g/n
Dimension	L x W x H: 18.00mm*20.00mm*2.45mm
RoHS	All hardware components are fully compliant with EU RoHS directive

1.4 Operating Conditions

Operating Voltage	3.3±10% Vdc
Operating Temperature	-10°C to +85°C
Storage Temperature	-40°C to +85°C

2 Wi-Fi RF Specification

2.1 2.4GHz RF Specification

Feature	**Description**			
WLAN Standard	IEEE 802.11 b/g/n Wi-Fi compliant			
Frequency Range	2.412～2.472GHz			
Number of Channels	**Wi-Fi:** USA/Canada: channel 1~11; Europe/China/Australia: channel 1~13			
Spectrum Mask	Min. b/g/n	Typ. b/g/n	Max. b/g/n	Unit b/g/n
1st side lobes(to fc ± 11MHZ)	-	-43/-30/-40	-	dBr
2st side lobes(to fc ± 22MHZ)	-	-52/-33/-58	-	dBr
Freq. Tolerance	-20/-20/-20	-	20/20/20	ppm

Test Items	**Typical Value**	**EVM**
Output Power	802.11b /11Mbps : 17dBm ± 2 dB	EVM ≤ -10dB
	802.11g /54Mbps : 15dBm ± 2 dB	EVM ≤ -25dB
	802.11n /MCS7 : 14dBm ± 2 dB	EVM ≤ -28dB

Test Items	**Test Value**	**Standard Value**
SISO Receive Sensitivity (11b,20MHz) @8% PER	- 1Mbps PER @ -94 dBm	≤-83 dBm
	- 2Mbps PER @ -92 dBm	≤-80 dBm
	- 5.5Mbps PER @ -89 dBm	≤-79 dBm
	- 11Mbps PER @ -87 dBm	≤-76 dBm
SISO Receive Sensitivity (11g,20MHz) @10% PER	- 6Mbps PER @ -89 dBm	≤-85 dBm
	- 9Mbps PER @ -88 dBm	≤-84 dBm
	- 12Mbps PER @ -87 dBm	≤-82 dBm
	- 18Mbps PER @ -86 dBm	≤-80 dBm
	- 24Mbps PER @ -84 dBm	≤-77 dBm
	- 36Mbps PER @ -80 dBm	≤-73 dBm
	- 48Mbps PER @ -77 dBm	≤-69 dBm
	- 54Mbps PER @ -74 dBm	≤-68 dBm
SISO Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0 PER @ -89 dBm	≤-85 dBm
	- MCS=1 PER @ -86 dBm	≤-82 dBm
	- MCS=2 PER @ -84 dBm	≤-80 dBm
	- MCS=3 PER @ -82 dBm	≤-77 dBm
	- MCS=4 PER @ -79 dBm	≤-73 dBm

	- MCS=5	PER @ -76 dBm	≤-69 dBm
	- MCS=6	PER @ -74 dBm	≤-68 dBm
	- MCS=7	PER @ -71 dBm	≤-67 dBm
Maximum Input Level	802.11b: -10 dBm		
	802.11g/n: -20 dBm		
Antenna Reference	PCB antenna with 0~2 dBi peak gain; External		

3 Power Consumption

Test mode	Current Value @3.3Vdc
TX	11M 138mA
	54M143mA
	11n-MCS7 144mA
	BLE 1M@15dBm 133mA
RX	11M 73mA
	54M 77mA
	11n-MCS7 77mA

4 Pin Assignments

4.1 Pin outline

< TOP VIEW >

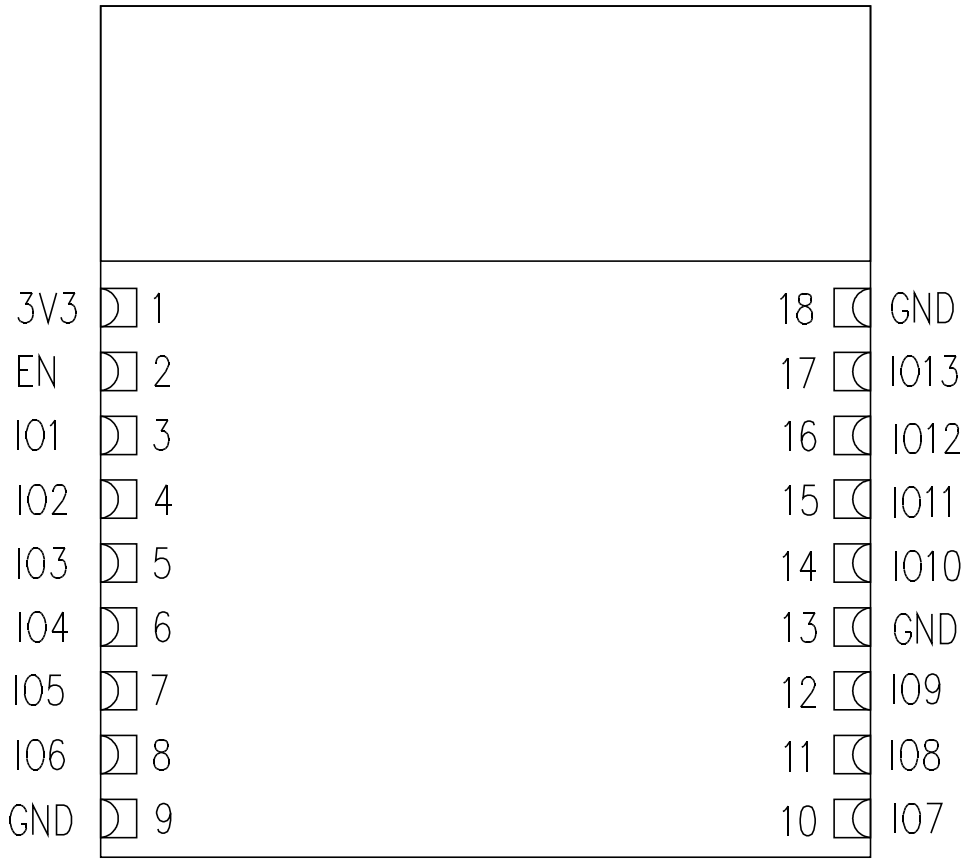


Figure 4-1 Pin Outline

4.2 Pin Definition

Pin#	Name	Type	Description	Voltage
1	3V3	P	3.3Vdc Power input	3.3V
2	EN	I	Enable chip. 1: Enable Chip, 0: Shut Down Chip. Default pull high	3.3V
3	IO1		GPIO Pin. The MUX Function can be referred to Pin Function Table	
4	IO2		GPIO Pin. The MUX Function can be referred to Pin Function Table	
5	IO3		GPIO Pin. The MUX Function can be referred to Pin Function Table	
6	IO4		GPIO Pin. The MUX Function can be referred to Pin Function Table	
7	IO5		GPIO Pin. The MUX Function can be referred to Pin Function Table	
8	IO6		GPIO Pin. The MUX Function can be referred to Pin Function Table	
9	GND		Ground connections	
10	IO7		GPIO Pin. The MUX Function can be referred to Pin Function Table	
11	IO8		Boot strap selection.Pin state sampled on rising edge of CHIP_EN. High: Boot from interface. Low: Boot from flash.	
12	IO9		GPIO Pin. The MUX Function can be referred to Pin Function Table	
13	GND		Ground connections	
14	IO10		GPIO Pin. The MUX Function can be referred to Pin Function Table	
15	IO11		GPIO Pin.　Chip Jtag TDO pin，Not recommended	
16	IO12		GPIO Pin. The MUX Function can be referred to Pin Function Table	
17	IO13		GPIO Pin. The MUX Function can be referred to Pin Function Table	

18	GND		Ground connections	

P: POWER I:INPUT O: OUTPUT

4.3 Pin Function Group Table

PIN		SDIO	SPI	UART0	UART2	I2C	PWM	ADC	JTAG
3	GPIO1	CMD	MOSIO/MII		UART0_CTS	SDA	PWM_CH1		TDI/TDO
4	GPIO0	CLK	MOSI /MISO		UART0_RTS	SCL	PWM_CH0		TMS/TCK
5	GPIO3	DAT1	SCLK		UART0_RXD	SDA	PWM_CH3		TDO/TDI
6	GPIO20		MOSI /MISO		UART1_RTS	SCL	PWM_CH0		TMS/TCK
7	GPIO16		MOSI /MISO	UART_TXD		SCL	PWM_CH1		TMS/TCK
8	GPIO7		SCLK	UART_RXD		SDA	PWM_CH2		TDO/TDI
10	GPIO4	DAT2	MOSI /MISO		UART1_RTS	SCL	PWM_CH4	ADC_CH1	TMS/TCK
11	GPIO12		MOSI /MISO		UART1_RTS	SCL	PWM_CH2	ADC_CH0	TMS/TCK
12	GPIO21		MOSIO/MII		UART1_CTS	SDA	PWM_CH1		TDI/TDO
14	GPIO14		SS		UART1_TXD	SCL	PWM_CH4	ADC_CH2 /DAC_B	TCK/TMS
15	GPIO5	DAT3	MISO /MOSI		UART1_CTS	SDA	PWM_CH0	ADC_CH4	TDI/TDO
16	GPIO8		MOSI /MISO		UART1_CTS	SDA	PWM_CH0	ADC_CH4	TDI/TDO
17	GPIO2	DAT0	SS		UART0_TXD	SCL	PWM_CH2		TCK/TMS

Note:

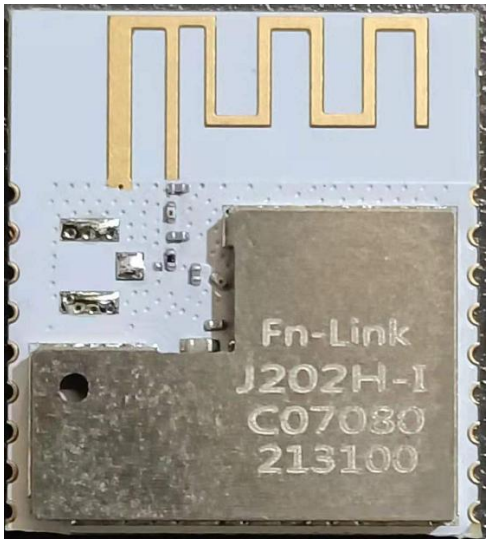
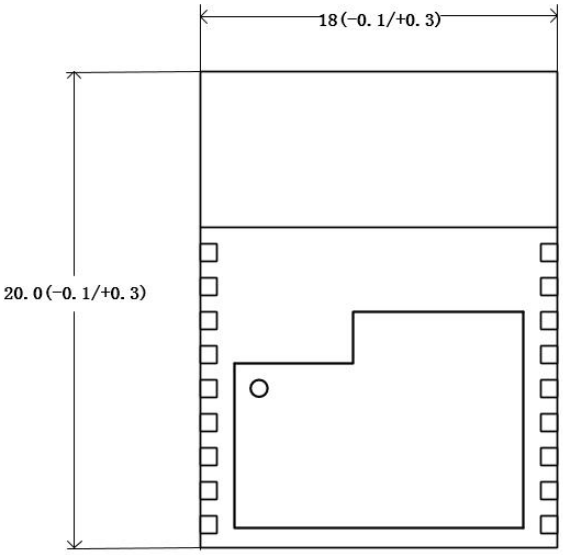
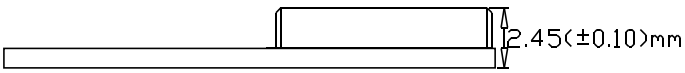
1, Pin7 is default configured as UART0_LOG_TXD, Pin8 is default configured as UART0_LOG_RXD, UART0 is used for firmware burning and print the booting log.

2, Pin11 is default configured as UART2_RXD, Pin12 is default configured as UART2_TXD, UART2 is used for AT communication, default baud rate is 115200.

5 Dimensions

5.1 Module Picture

<table>
<tr><td>L x W: 18 x 20 (+0.3/-0.1) mm
On board PCB antenna:
FGJ202HIXX-00

 
</td><td> 
</td></tr>
<tr><td>H: 2.45 (±0.10) mm</td><td> 
</td></tr>
<tr><td>Weight</td><td>TDB</td></tr>
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5.2 Physical Dimensions

(unit: mm)

< TOP VIEW >

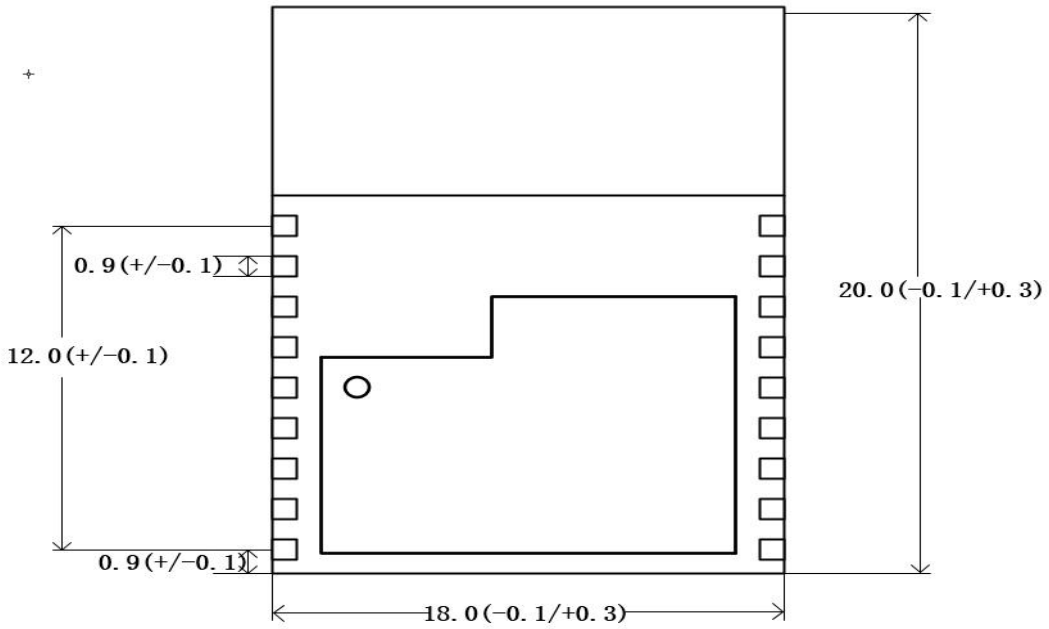


Figure 5-1 Physical Dimensions

5.3 Layout Recommendation

(unit: mm)

< TOP VIEW >

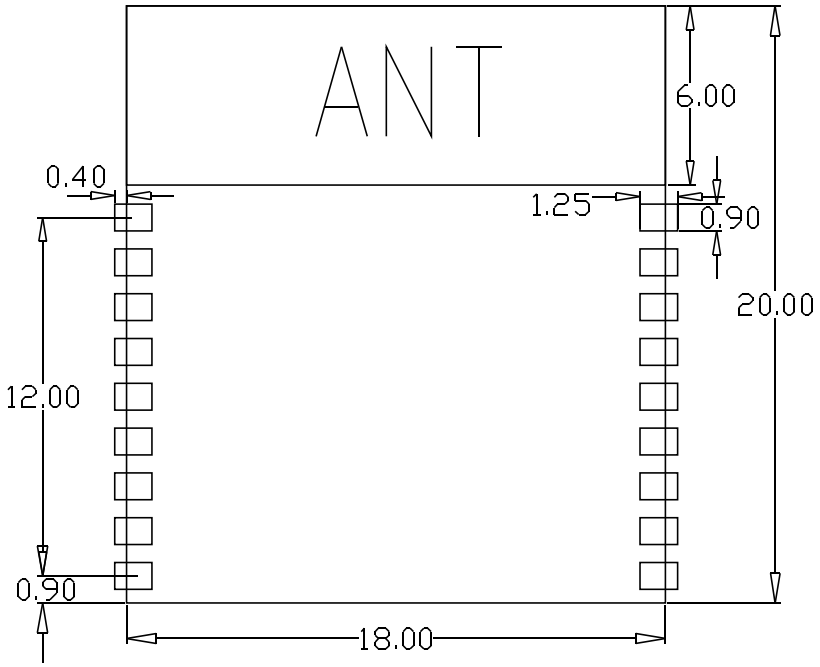


Figure 5-2 Layout recommendation

5.4 RF connector for external antenna

Unite:mm

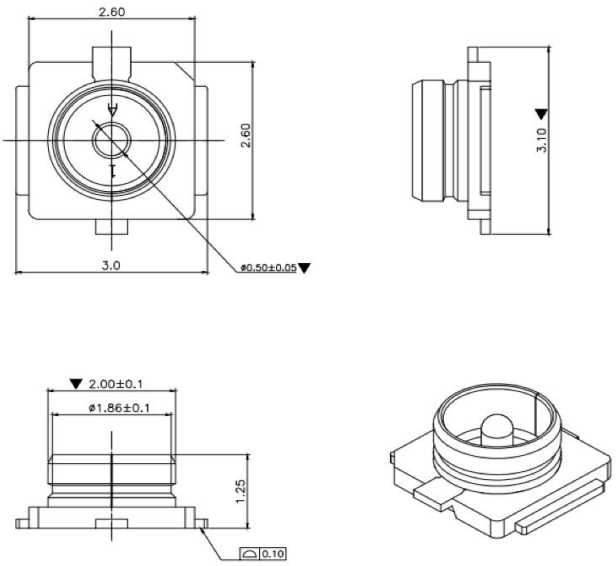


Figure 5-3 RF connector for external antenna

6 Reference Design

6.1 Schematic reference design

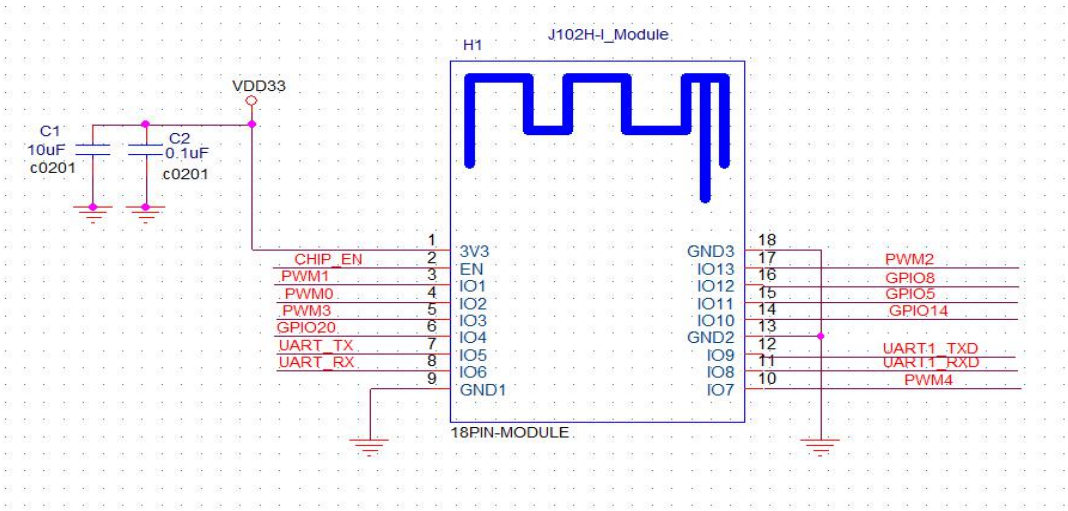


Figure 6-1 Reference Schematic

Note:

Please place C1,C2 close to PIN 1.

It is recommended have power supply current greater than 500mA for the module.

PIN16 GPIO8 Do not pull this pin up

6.2 Antenna clearance area requirements

When using PCB antenna on Wi-Fi module, make sure the distance between PCB on motherboard and other metal devices is at least 16mm.The shaded areas in the figure below need to be marked away from metal devices, sensors, interference sources, and other materials that may interfere with the signal.

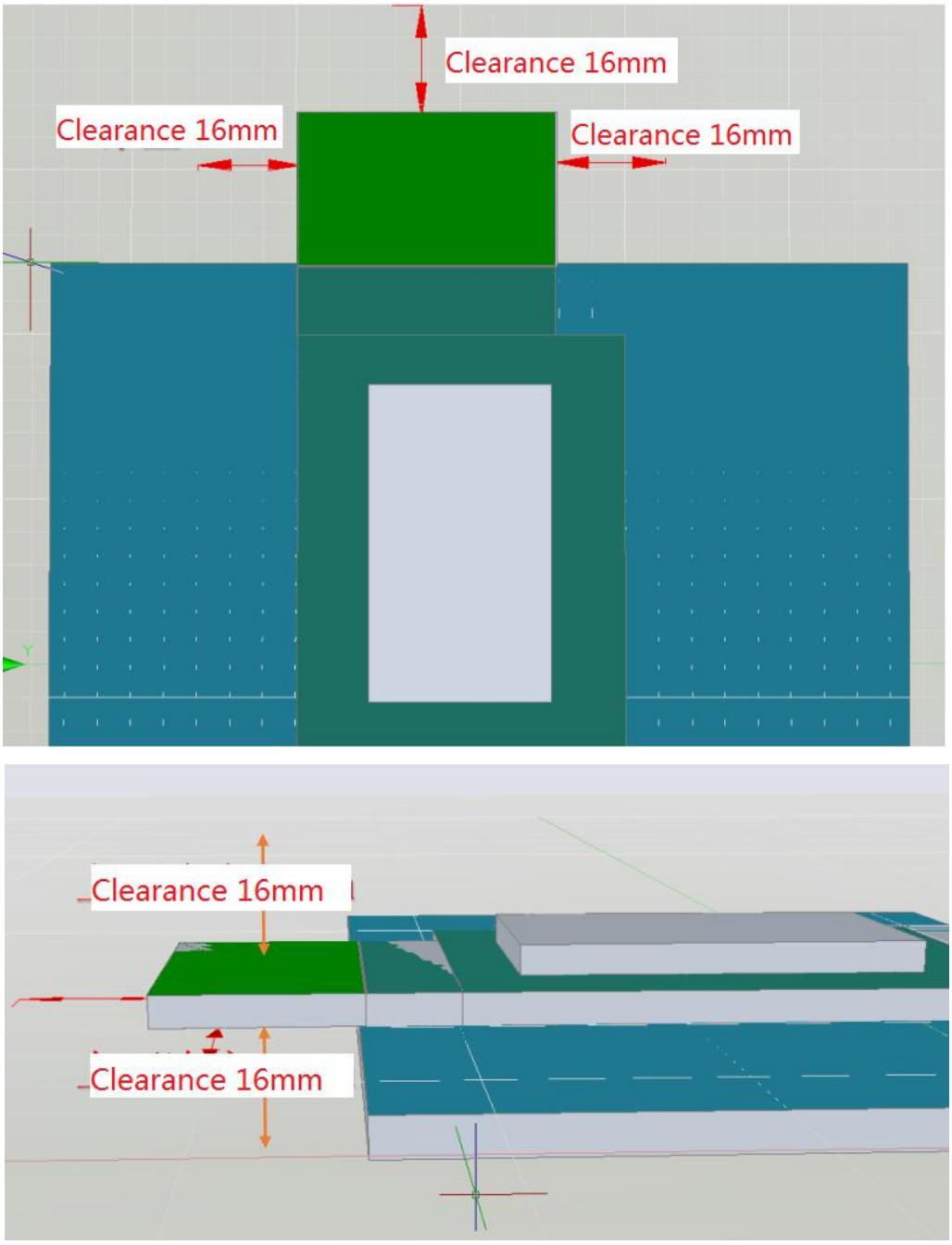


Figure 6-2 Antenna clearance reference

7 Ordering Information

Part NO.	Description
FGJ202HIXX-00	BL602C-20-Q2I, 802.11b/g/n, 1T1R, UART/GPIO/I2C/PWM/SPI/SDIO/I2S, PCB ANT, 18*20mm, PCB V1.0

8 The Key Material List

Item	Part Name	Description	Manufacturer
1	Crystal	3225 40MHz 10ppm	ECEC, TKD, Hosonic, JWT, TXC
2	Chipset	BL602C-20-Q2I	博流
3	PCB	FR4, 2 LAYER, GREEN	XY-PCB, GDKX, Sunlord, SLPCB

9 Recommended Reflow Profile

Refer to IPC/JEDEC standard.
Peak Temperature: <250°C
Number of Times: ≤2 times

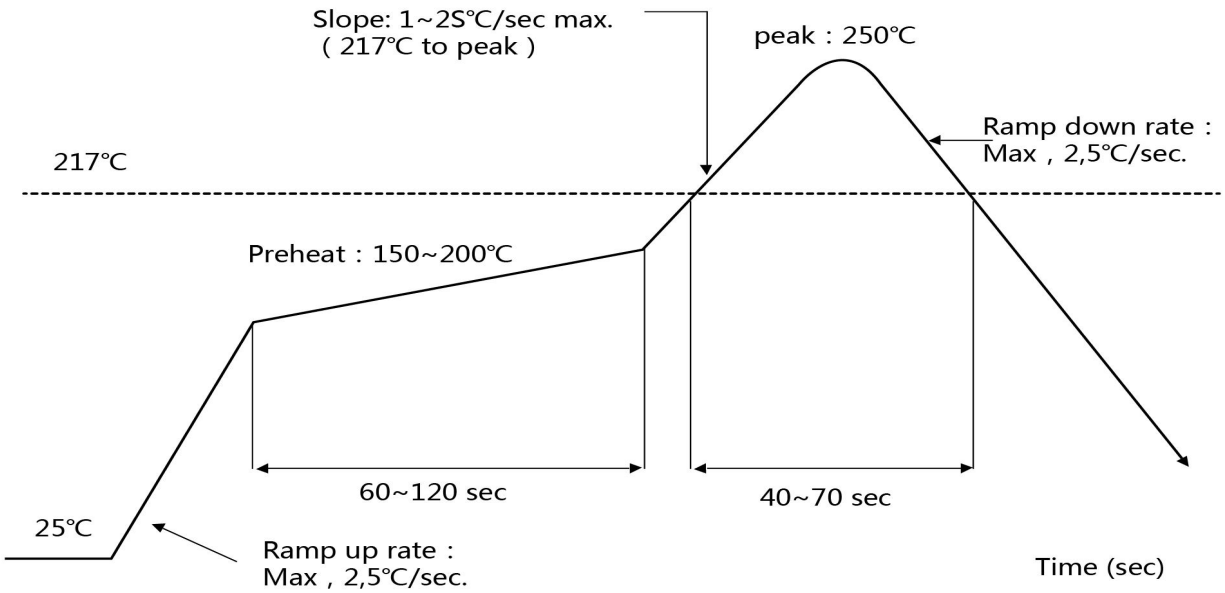


Figure 9-1 Reference reflow profile

10 Package Information

10.1 Reel

A roll of 800pcs

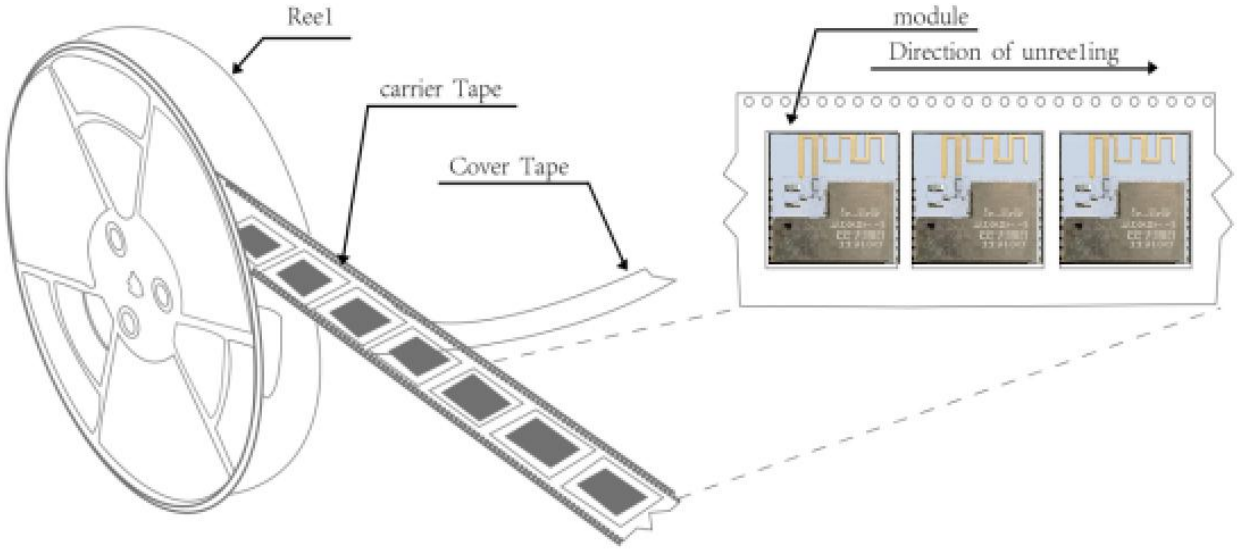


Figure 10-1 Package reel Reference

10.2 Carrier Tape Detail

ITEM	W	A0	B0	D	E	F	F1	K0	P0	P2	P	T
DIM	32	18.40	20.30	1.5	1.75	14.20	28.4	3.50	4.0	2.0	24.0	0.30
TOLE	+0.3 -0.3	±0.15	±0.15	+0.1 -0.0	±0.1	±0.15	±0.10	±0.10	±0.1	±0.15	±0.1	±0.05

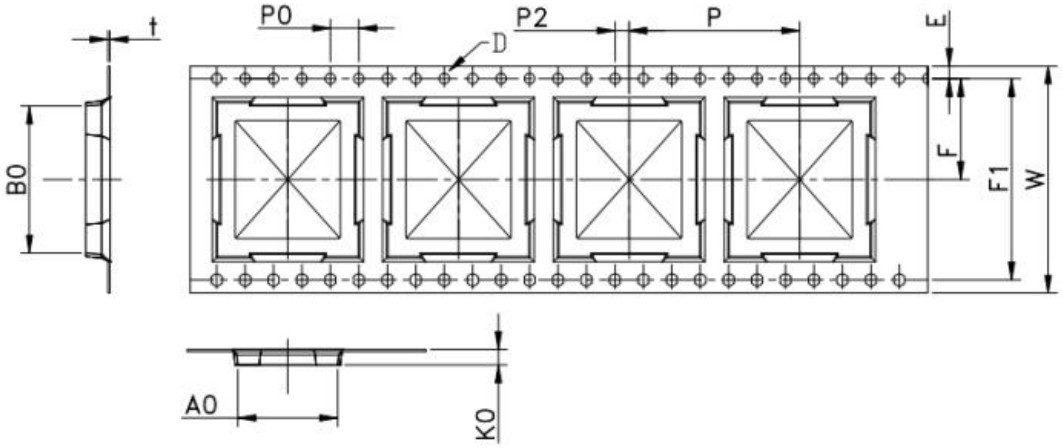


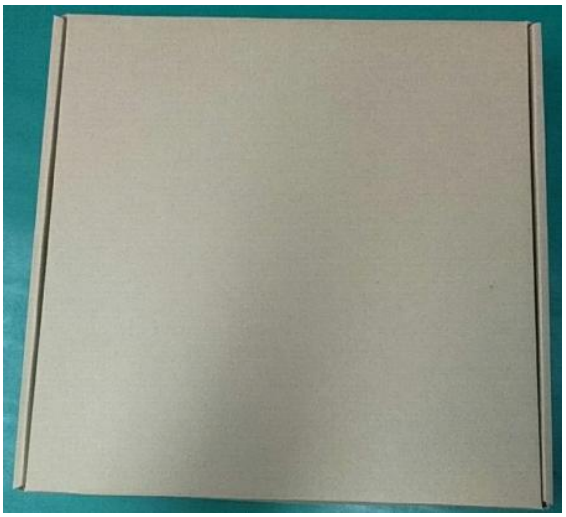
Figure 10-2 Carrier tape detail

10.3 Packaging Detail

the take-up package

Using self-adhesive tape
Size of black tape:44mm*20.2m　　the cover tape :37.5mm*20.2m
Color of plastic disc: blue
A roll of 800pcs

NY bag size:415mm*450mm



size ： 350X350X35mm

The packing case size: 360X210X370mm

10.4 Moisture Sensitivity

The Modules is a Moisture Sensitive Device level 3, in according with standard IPC/JEDEC J-STD-020, take care all the relatives requirements for using this kind of components.

Moreover, the customer has to take care of the following conditions:

a) Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH)

b) Environmental condition during the production: 30°C / 60% RH according to IPC/JEDEC J-STD-033A paragraph 5

c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition

d) “IPC/JEDEC J-STD-033A paragraph 5.2” is respected

e) Baking is required if conditions b) or c) are not respected

f) Baking is required if the humidity indicator inside the bag indicates 10% RH or more