PAW3020J1: Optical Finger Navigation (OFN) Module

General Description

The PAW3020J1 is a small form factor (SFF) Optical Finger Navigation (OFN) module. It is for finger control of the in-vehicle infotainment system. It is capable of finger motion speed detection – up to 14 ips on small area of touch cover window. The XY navigation output comes with finger movement.

In addition, it has an on-chip oscillator and integrated LED to minimize external components. There are no moving parts, thus provide high reliability and less maintenance for the end users. Precision optical alignment is also not required, facilitating high volume assembly. The chip is programmed via registers through either I2C or SPI interface port. It is packaged into an 18-pin FPC module for ease of assembly via ZIF connector.

Key Features

- Automotive grade device
- Compliant to AEC-Q100 grade 3
- Precise optical motion estimation technology
- Motion detection up to 14 inches/sec
- Resolution : 200 ~ 2000 CPI (counts per inch)
- Operation mode
  - Free navigation mode
  - Directional modes - 2 / 4 / 8 directions
- Hardware reset for flexible system control
- Sunlight resistant

Applications

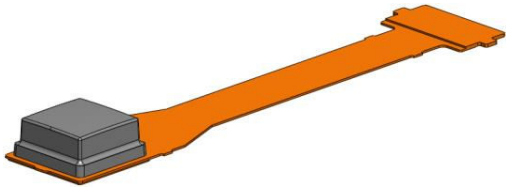
- In-Vehicle Infotainment System
- Finger navigation in HID

Key Parameters

Parameter	Value
Operating Temperature	-40 ~ 85°C
Supply Voltage	VDDM : 3.0V ~ 3.6V VDDIO : 1.62 ~ 3.6V VDDIO ≦ VDDM
Interface	4-wire SPI/I2C
Tracking speed	Max 14 inches/sec
CPI Resolution	200/400/500/600/800 /1000(default)/1200/1600 /2000 CPI
Operating Current **Note:** Including LED current	Typical : 3.5mA (with I/O toggle) W/O finger touch: 11mA Sleep mode: 2mA
Package	18-pin FPC module with 0.5mm contact pitch

Ordering Information

Part Number	Part Description
PAW3020J1	Optical Finger Navigation Module



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1.0 Introduction

1.1 Overview

The PAW3020J1 is a FPC module consists of OFN chip, optical lens and lens cover. The OFN chip is a high performance and low power CMOS-process optical chip with integrated DSP serving as a non-mechanical motion estimation engine for finger touch navigation. An infrared LED is integrated in the OFN module, serving as the light source. It is based on optical navigation technology which measures variation in position by optically acquiring sequential surface images (frames) and mathematically determining the direction and magnitude of movement. The movement of △X and △Y are available in the registers accessed via serial port.

The word “module” instead of PAW3020J1, is used in this document.

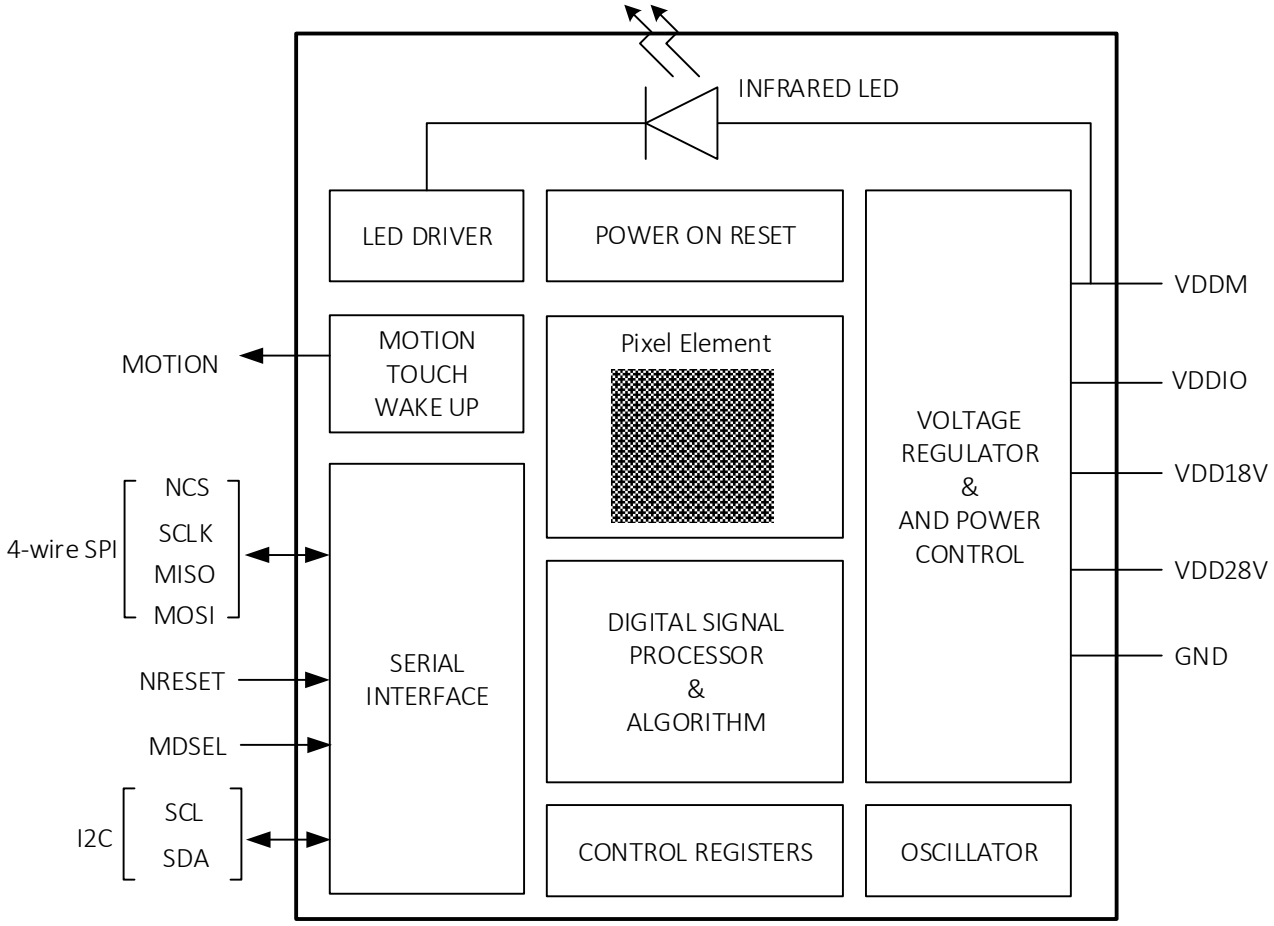
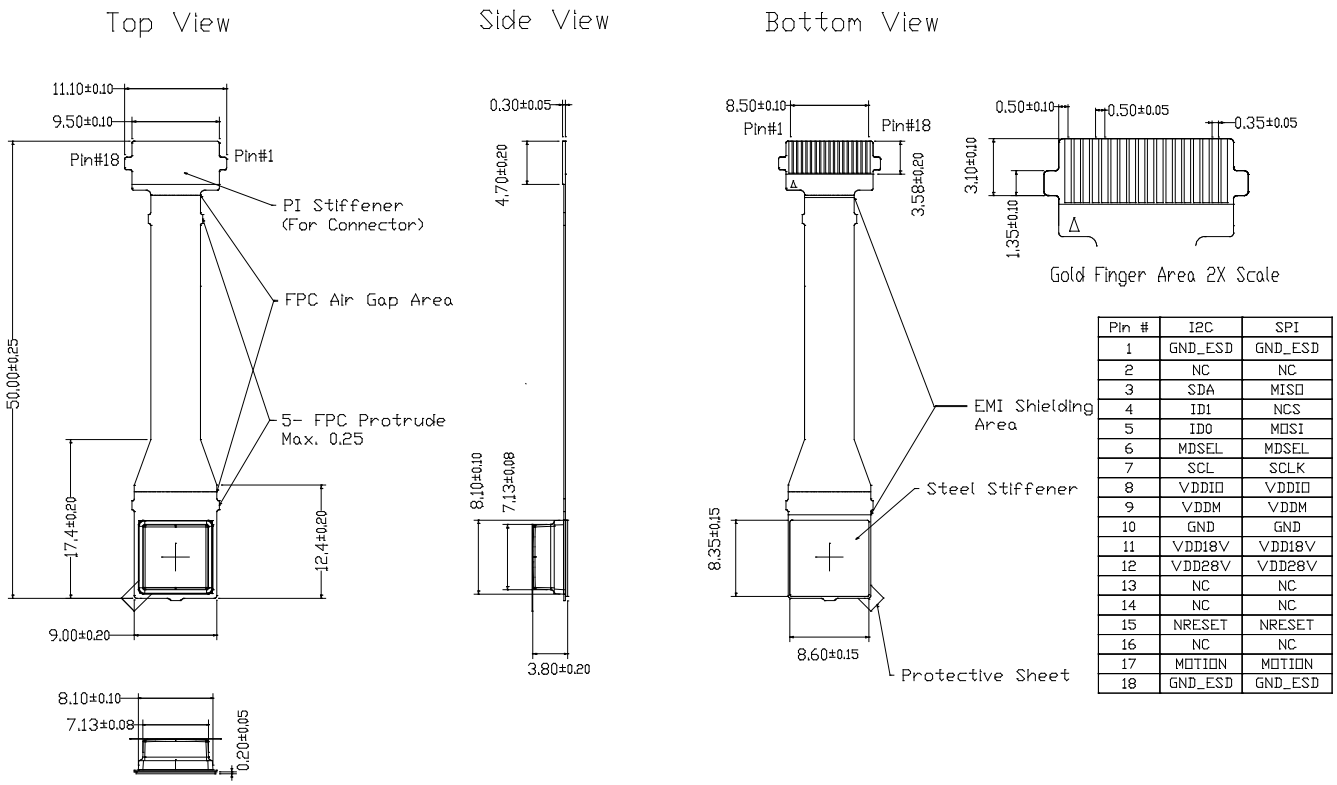


Figure 1. Block Diagram

1.2 Signal Pin Definition

Pin #	Signal Name		Type	Pin Definition
	I2C	4-wire SPI		
1	GND_ESD	GND_ESD	GND	Ground for enhancing ESD protection.
2	NC	NC	NC	No connection
3	SDA	MISO	I/O	SDA pin for I2C interface MISO pin for 4-wire SPI interface
4	ID1	NCS	IN	Slave ID selection for I2C interface NCS pin for 4-wire SPI interface (low active)
5	ID0	MOSI	IN	Slave ID selection for I2C interface MOSI pin for 4-wire SPI interface
6	MDSEL	MDSEL	IN	To select I2C or 4-wire SPI interface Low : I2C interface High : 4-wire SPI interface
7	SCL	SCLK	IN	Clock pin for I2C / 4-wire SPI
8	VDDIO	VDDIO	PWR	I/O power supply (1.62V ~ 3.6V) VDDIO ≦ VDDM
9	VDDM	VDDM	PWR	Main power supply (3.0V ~ 3.6V)
10	GND	GND	GND	Ground
11	VDD18V	VDD18V	PWR	Internal regulator output and should be connected a 0.22uF capacitor to ground
12	VDD28V	VDD28V	PWR	Internal regulator output and should be connected a 0.1uF capacitor to ground
13	NC	NC	NC	No connection
14	NC	NC	NC	No connection
15	NRESET	NRESET	IN	System reset (low active)
16	NC	NC	NC	No connection
17	MOTION	MOTION	OUT	Motion interrupt (low active)
18	GND_ESD	GND_ESD	GND	Ground for enhancing ESD protection.

2.0 Mechanical Specifications



Pin #	I2C	SPI
1	GND_ESD	GND_ESD
2	NC	NC
3	SDA	MISO
4	ID1	NCS
5	ID0	MOSI
6	MDSEL	MDSEL
7	SCL	SCLK
8	VDDIO	VDDIO
9	VDDM	VDDM
10	GND	GND
11	VDD18V	VDD18V
12	VDD28V	VDD28V
13	NC	NC
14	NC	NC
15	NRESET	NRESET
16	NC	NC
17	MOTION	MOTION
18	GND_ESD	GND_ESD

Figure 2. OFN Module Outline Drawing

3.0 Electrical Specifications

3.1 Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
T_{STG}	Storage Temperature	-40	105	°C	
TA	Operating Temperature	-40	85	°C	
VDDM	DC Supply Voltage	3.0	3.6	V	VDDIO ≦ VDDM
VDDIO	DC Input Voltage	1.62	3.6	V	All I/O pin, VDDIO ≦ VDDM
ESD_{I2C_A}	Air ESD for I2C		+/- 25	kV	Air ESD for I2C interface
ESD_{I2C_C}	Contact ESD for I2C		+/- 15	kV	Contact ESD for I2C interface
ESD_{4SPI_A}	Air ESD for 4SPI		+/- 25	kV	Air ESD for 4SPI interface
ESD_{4SPI_C}	Contact ESD for 4SPI		+/- 15	kV	Contact ESD for 4SPI interface

3.2 Recommended Operating Conditions

Table 2. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Notes
T_A	Operating Temperature	-40	-	85	°C	
VDDM	Power Supply Voltage	3.0	3.3	3.6	V	VDDIO ≦ VDDM
VDDIO	IO Supply Voltage	1.62	3.3	3.6	V	VDDIO ≦ VDDM
V_{Npp}	Supply Noise	-	-	100	mV	Peak to peak within 10k – 80 MHz
R	Resolution	200	1000	2000	CPI	
SCK	SPI Clock Frequency	-	-	1	MHz	
	I2C Clock Frequency	-	-	400	kHz	
S	Speed	-	-	14	ips	Inches per second

3.3 AC Electrical Characteristics

Electrical Characteristics are defined under recommended operating conditions. Typical values at 25 °C, VDDIO = 3.3V for 3.3V application.

Table 3. AC Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
t_{PDR}	PD Pulse Register	-	-	800	us	2 frames time maximum after setting ***PD_enh*** bit in the ***Configuration*** register @ half full frame rate (refer to Figure 15. Power-down).
t_{delay}	Address and data delay time	2.75			us	refer to Figure 7.
t_r , t_f	Rise and Fall Times: SDA		-	300	ns	
t_{reset}	Data ready time after Reset	1			ms	Data ready time after SW or HW Reset

3.4 DC Electrical Characteristics

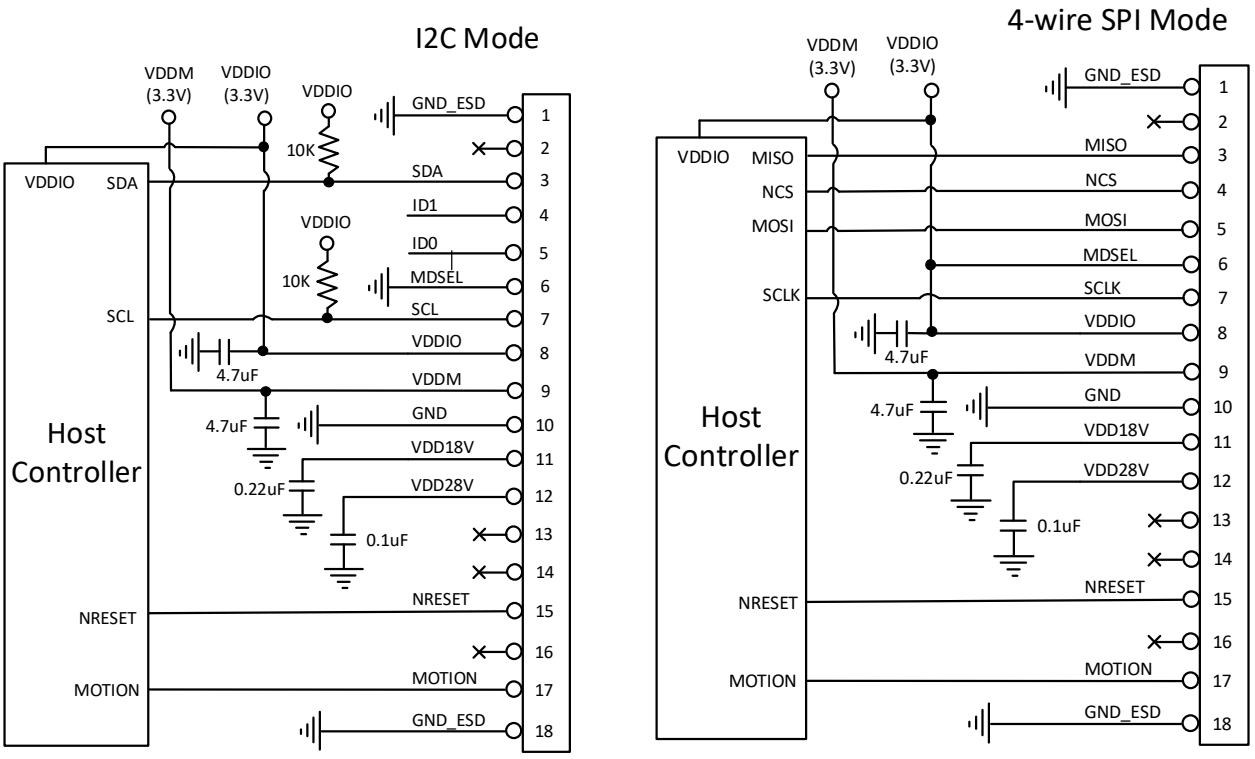
Electrical Characteristics are defined under recommended operating conditions. Typical working temperature is 25 °C. VDDIO=3.3V+/-10%.

Table 4. DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
I_{DDN}	Supply Current for Chip OFM Moving (Normal)	-	1.7		mA	No including LED current, w/o interface I/O toggle
I_{LEDN}	Supply Current for LED OFM Moving (Normal)	-	1.8		mA	@LED_Step = 13
I_{N_FINGER}	Supply Current W/O finger touch		11		mA	
I_{DDPD}	Supply Current for Chip (Power Down)	-	10	-	uA	
I_{sleep}	Supply Current for whole module at sleep mode		2		mA	
V_{IH}	Input Voltage HIGH	0.8*VDDIO	-		V	@VDDIO = 3.3V; @VDDIO = 1.62V
V_{IL}	Input Voltage LOW			0.2*VDDIO	V	@VDDIO = 3.3V; @VDDIO = 1.62V

4.0 System Design

4.1 Application Circuit



ID0	ID1	7-bit slave ID (hex)
0	0	33
0	1	37
1	0	53
1	1	57

Figure 3. Application Circuits of OFN Modules

5.0 Power-up Sequence Requirements

If the VDDIO and VDDM for the chip are not sourced from the same power supplies input, a power-up sequence is applicable on these two power inputs to avoid excessive current leakage or occurrence of unexpected system instability happening on the chip.

1. VDDM must be powered up first or at the same time with VDDIO ($T1 \geq 0$). VDDIO can never be powered up earlier than VDDM.
2. MDSEL must toggle at the same time with VDDIO.
3. NRESET must power up later than VDDM ($T2 \geq 0$).

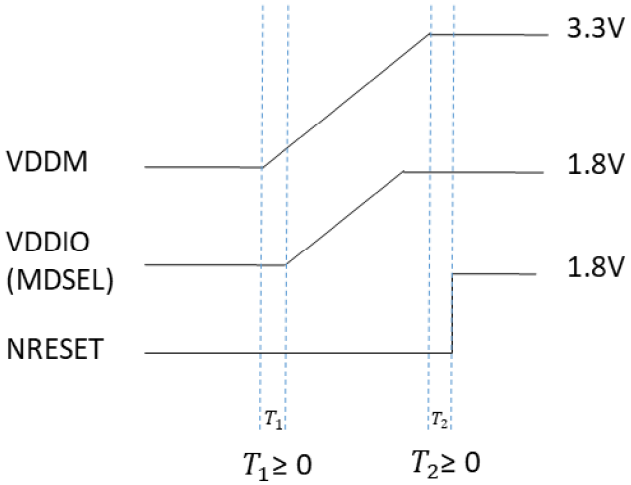


Figure 4. Power sequence

6.0 Serial Interface

The synchronous serial port is used to set and read parameters in the chip.

6.1 Four-Wire SPI Interface

- NCS: Chip select line, low active (Generally named SPI_CS).
- SCK: Serial clock line, generated by the host controller.
- MOSI: Serial data line, used to write data to chip.
- MISO: Serial data line, used to read data from chip.

6.1.1 Transmission Protocol

The transmission protocol is a 4-wire link, half duplex protocol between the micro-controller and the chip. All data changes on MOSI/MISO are latched at SCK rising edge. The host controller always initiates communication and the chip never initiates data transfers.

The transmission protocol consists of the two operation modes:

- Write Operation.
- Read Operation.

Both of the two operation modes consist of two bytes. The first byte contains the address (seven bits) and has a bit 7 as its MSB to indicate data direction. The second byte contains the data.

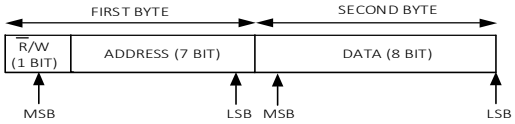


Figure 5. Transmission Protocol

6.1.2 Write Operation

A write operation, which means that data is going from the host controller to the chip, is always initiated by the controller and consists of two bytes. The first byte contains the address (seven bits) and has a "1" as its MSB to indicate data direction. The second byte contains the data. The transfer is synchronized by SCK. The controller changes MOSI at SCK falling edges. The chip reads MOSI at SCK rising edges.

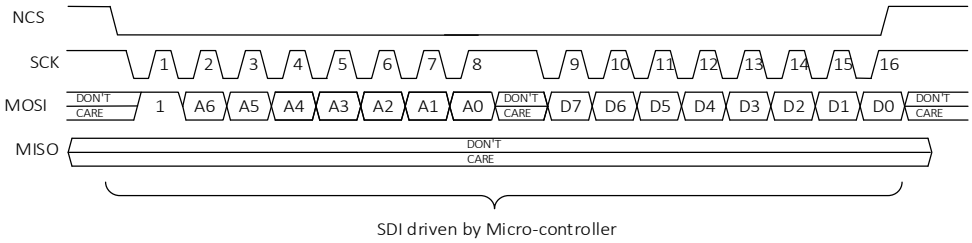


Figure 6. Write Operation

6.1.3 Read Operation

A read operation, which means that data is going from the chip to the controller, is always initiated by the HOST controller and consists of two bytes. The first byte contains the address, is written by the controller, and has a "0" as its MSB to indicate data direction. The second byte contains the data and is driven by the chip. The transfer is synchronized by SCK.

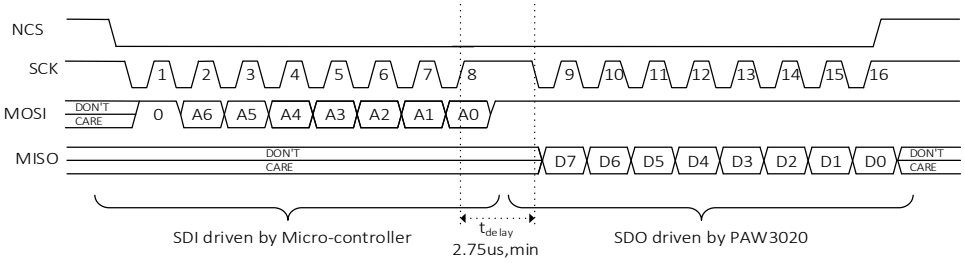


Figure 7. Read Operation

6.1.4 Timing Specifications

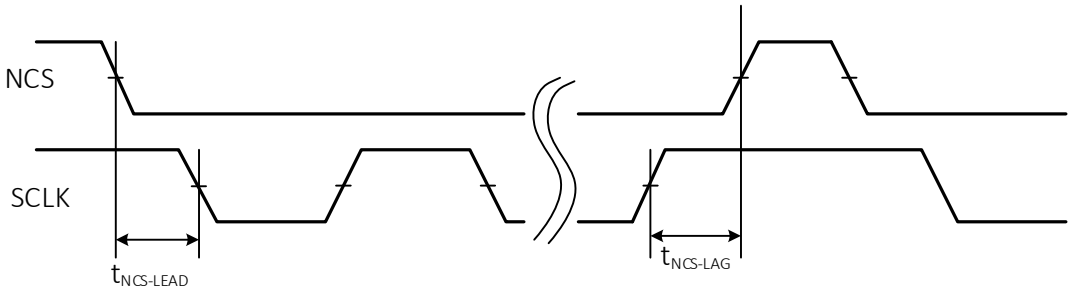


Figure 8. NCS vs SCLK Timing Requirement

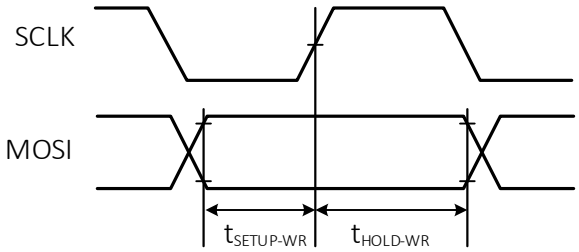


Figure 9. MOSI setup and hold time during write operation

Table 5. SPI Timing Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
SCLK frequency	F_{SCLK}	-	-	1	MHz	SPI max. operation frequency
NCS Enable Lead Time	$t_{NCS-LEAD}$	2.75	-	-	µs	From NCS falling to first SCLK falling
NCS Enable Lag Time	$t_{NCS-LAG}$	2.75	-	-	us	From Last SCLK rising to NCS rising
SCLK delay for Data Preparation	t_{delay}	2.75	-	-	us	The min. time between the rising of 8^{th} SCLK and the falling of 8^{th} SCLK
MOSI Write Setup Time	$t_{SETUP-WR}$	1/8T	-	-	ns	SDA data valid before SCLK rising
MOSI Write Hold Time	$t_{HOLD-WR}$	1/4T	-	-	ns	SDA data valid after SCLK rising
MOSI Read Hold Time	$t_{HOLD-RD}$	-	3	-	us	SDA data valid after SCLK rising
MOSI Rise Time	t_{SDA-R}	-	30	-	ns	@C_L = 30 pF
MOSI Fall Time	t_{SDA-F}	-	30	-	ns	@C_L = 30 pF

Note: All the parameters are tested under operating conditions: V_{DDM} = 3.3V and T_A = 25°C. T = SPI clock (SCK)

6.2 I2C Interface

- **SCK:** Serial clock line, generated by the host controller (Generally named SCL).
- **SDA:** Serial data line, used to read data from chip (Generally named SDA).

PAW3020J1 supports I2C bus transfer protocol and acts as slave device. The 7-bits selectable slave address is depending on ID0 and ID1 input pin state and supports receiving / transmitting speed as maximum 400kHz.

Table 6. I2C Slave Address

ID0	ID1	7-bit slave address (hex)
Low	Low	33
Low	High	37
High	Low	53
High	High	57

6.2.1 I2C Bus Overview

- Only two wires SDA (serial data) and SCK (serial clock) carry information between the devices connected to the I2C bus. Normally both SDA and SCK lines are open collector structure and pulled high by external pull-up resistors.
- Only the master can initiate a transfer (start condition), generates clock signals, and terminates a transfer (stop condition).
- Start and stop condition: A high to low transition of the SDA line while SCK is high defines a start condition. A low to high transition of the SDA line while SCK is high defines a stop condition. Please refer to Figure 10.
- Valid data: The data on the SDA line must be stable during the high period of the SCK clock. Within each byte, MSB is always transferred first. Read / Write control bit is the LSB of the first byte. Please refer to Figure .
- Both the master and slave can transmit and receive data from the bus.
- Acknowledge: The receiving device should pull down the SDA line during high period of the SCK clock line when a complete byte was transferred by transmitter. In the case of a master received data from a slave, the master does not generate an acknowledgment on the last byte to indicate the end of a master read cycle.

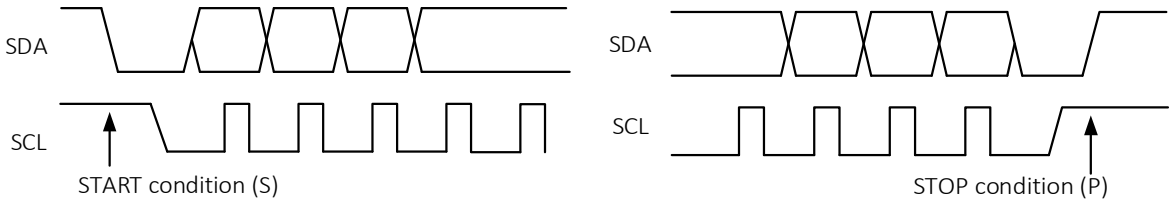


Figure 10. Start and Stop conditions

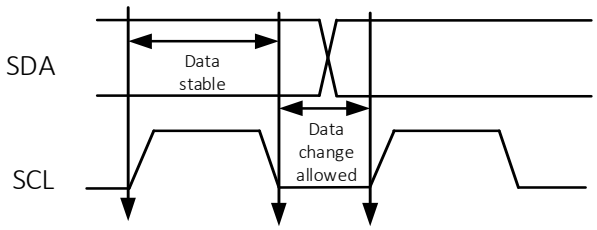


Figure 11. Valid Data

6.2.2 Data Transfer Format

6.2.2.1 Master Transmits Data to Slave (Write Cycle)

S : Start.

A : Acknowledge by salve.

P : Stop.

RW : The LSB of 1ST byte to decide whether current cycle is read or write cycle.
RW = 1 – Read cycle, RW = 0 – Write cycle.

ADDRESS : The address values of PAW3020J1 internal control registers.

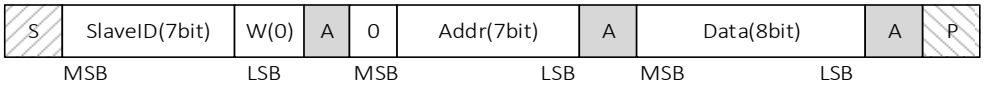


Figure 12. Write cycle

During write cycle, the master generates start condition and then places the 1st byte data that are combined slave ID (7 bits) with a read / write control bit to SDA line. After slave (PAW3020J1) issues acknowledgment, the master places 2nd byte (Address) data on SDA line. Again follow the PAW3020J1 acknowledgment, the master places the 8 bits data on SDA line and transmit to PAW3020J1 control register (address was assigned by 2nd byte). After PAW3020J1 issue acknowledgment, the master can generate a stop condition to end of this write cycle.

6.2.2.2 Slave Transmits Data to Master (Read Cycle)

During read cycle, the master generates start condition and then places the 1st byte data that are combined slave ID (7 bits) with a read / write control bit to SDA line. After issue acknowledgment, 8 bits DATA was also placed on SDA line by PAW3020J1. The 8 bits data was read from PAW3020J1 internal control register that address was assigned by previous write cycle. If the host intends to terminate the transfer, it responds with not acknowledge (NA, SDA = 1), and then drives SDA to generate a STOP condition.

Figure 13. Read cycle

6.2.3 I2C Bus Timing

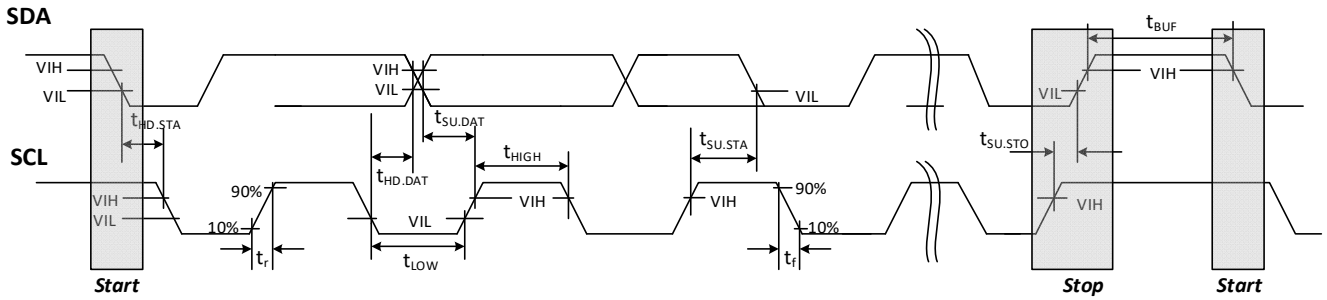


Figure 14. I2C Bus Timing

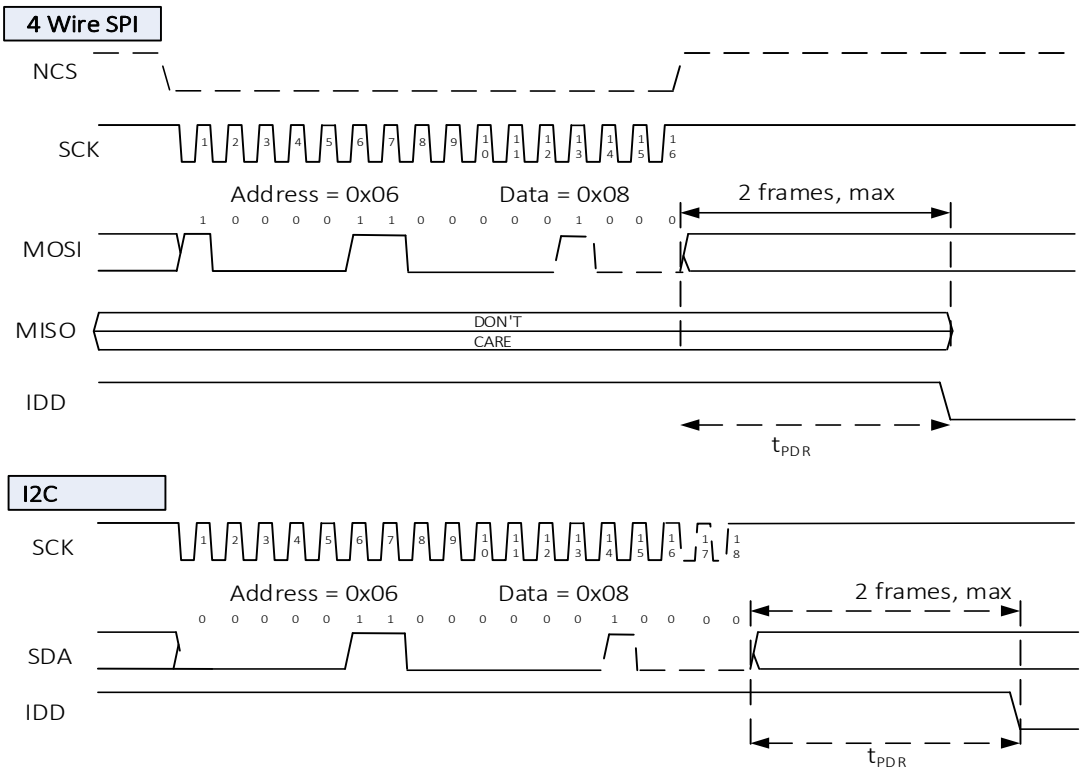
Table 7. I2C Bus Timing Specification

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
SCL clock frequency.	F_{scl}	-	-	400	kHz	
Hold time for Start/Repeat Start. After this period, the first clock pulse is generated.	$t_{HD.STA}$	0.6	-	-	µs	
Set-up time for a repeated Start.	$t_{SU.STA}$	0.6	-	-	µs	
Low period of SCL clock.	t_{LOW}	1.3	-	-	µs	
High period of SCL clock.	t_{HIGH}	0.6	-	-	µs	
Data hold time.	$t_{HD.DAT}$	0	-	-	µs	
Data set-up time.	$t_{SU.DAT}$	250	-	-	ns	
Rise time of both SDA and SCL signals.	t_r	-	-	300	ns	
Fall time of both SDA and SCL signals.	t_f	-	-	300	ns	
Set-up time for STOP condition.	$t_{SU.STO}$	0.6	-	-	µs	
Bus free time between a STOP and START.	t_{BUF}	1.3	-	-	µs	

7.0 Functional Operation

7.1 Software Power Down Mode

The chip can be placed in a power-down mode by setting ***PD_enh*** bit in the ***Configuration*** register via a serial port write operation. After setting the ***Configuration*** register, wait at most 2 frames times. To get the chip out of the power down mode, clear ***PD_enh*** bit in the ***Configuration*** register via a serial port write operation. In the power down mode, the serial interface still can read/write normally. For an accurate report after leave the power down mode, wait about 3ms before the HOST controller is able to issue any write/read operation to the chip.



Configuration Register Writing Operation

Figure 15. Power-down

7.2 Reading the Motion, Direction Data and calculating Firmware Touch Value

- Whenever the chip detects the occurrence of motion, the detected motion data (X-movement and Y-movement) is accumulated and stored in chip's internal buffer.
- The host controller can read out direction value through register Delta_X, Delta_Y and Direction_Value (address 0x03, 0x04, 0x34).
- Before reading the motion data through these registers, do ensure to read register Motion_Status (address 0x02) first to check if the MOTION bit (bit 7) is 1.
- If the MOTION bit is 1, the data in register Delta_X, Delta_Y and Direction_Value is valid, otherwise it is invalid.
- If firmware touch function is required, read out the corresponding registers and calculate the Firmware touch value as the sample code which described in PAW3020 Application Note.
- The host controller can use the following polling mode to read out the chip motion data.
  - By reading and checking register Motion_Status (address 0x02) periodically, the host controller can get the motion data in a simple way through I^2C or SPI interface.
  - Be noticed that the 2ms shown in the flowchart below is a recommended value. The delay time might depend on the capability of the host controller to cater for the need of different applications.

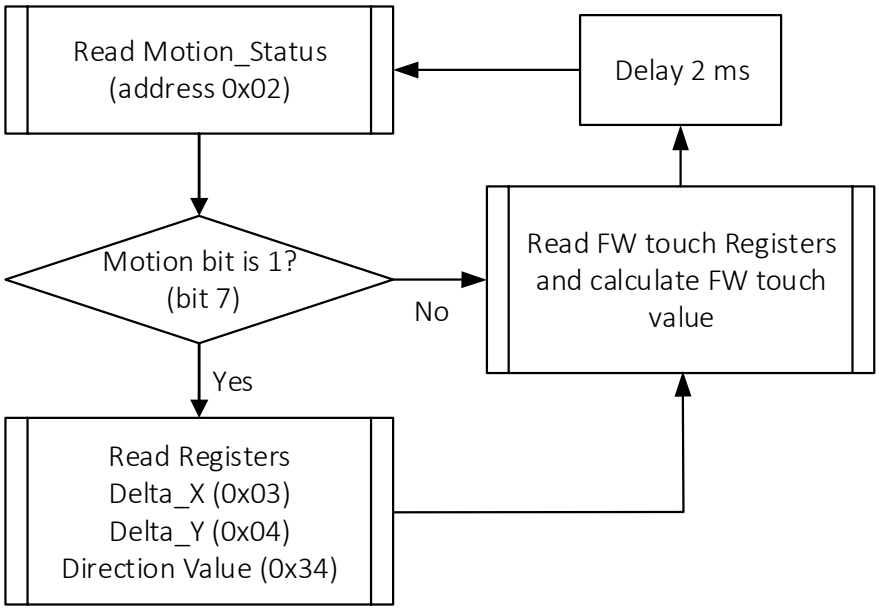


Figure 16. Read Direction Data with Polling Mode