2LAN500 - Module

DATA SHEET

22. Februar 2017

Version 1.4

ADATIS

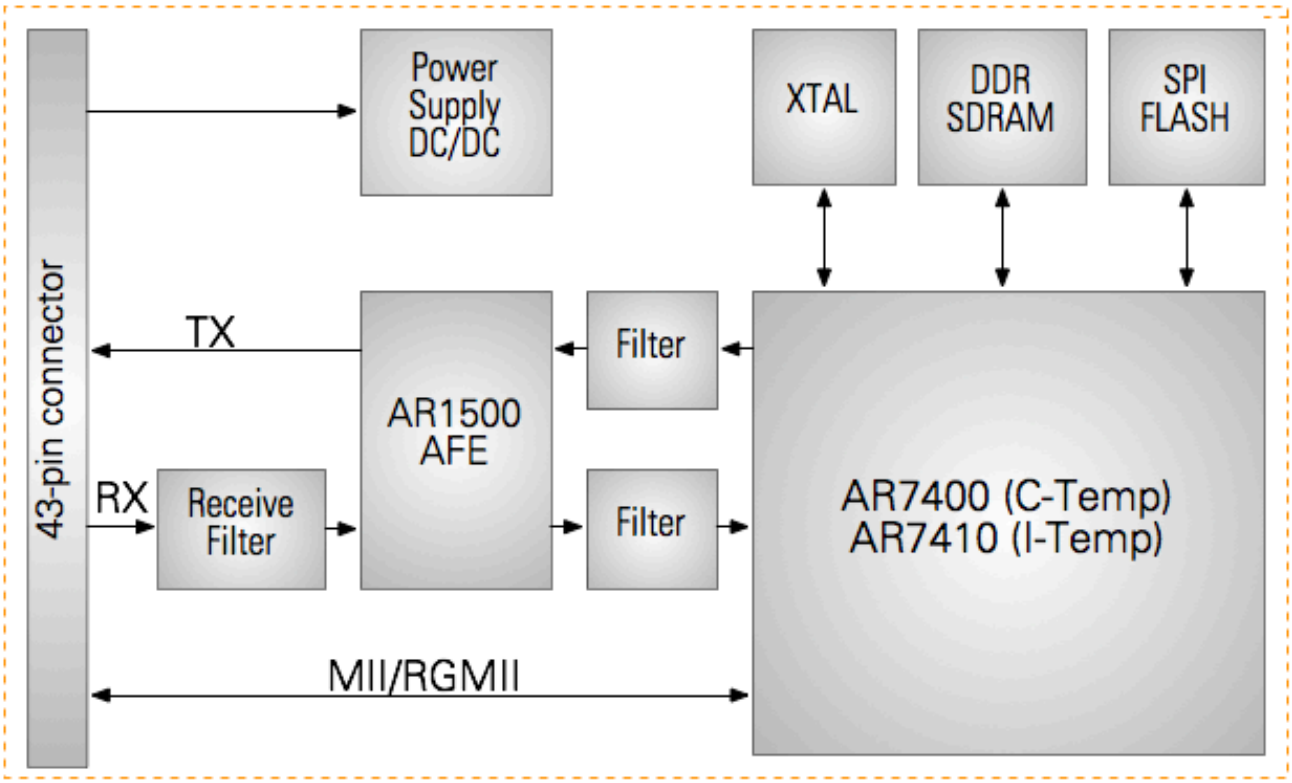
VERSION HISTORY

Version	Date	Comment
1.0	04.08.2015	Initial version
1.1	12.05.2016	Mechanical specification in section 8.5 updated
1.2	01.09.2016	Changed connector in section 8.5 for horizontal version
1.3	25.11.2016	Added lead size for the connectors in section 8.5
1.4	22.02.2017	Changed transformer datasheet in section 9.1 to type TMS61518CS

Contents

1. Ordering Information

Ordering Code	Description
2LAN500-HC	**H**orizontal Module, **C**ommercial Temperature, MII-Interface
2LAN500-VC	**V**ertical Module, **C**ommercial Temperature, MII-Interface
2LAN500-HI	**H**orizontal Module, **I**ndustrial Temperature, RGMII-Interface
2LAN500-VI	**V**ertical Module, **I**ndustrial Temperature, RGMII-Interface



2. Description

The 2LAN500 PLC-Module is an integrated device for transmitting and receiving data over the power line or any other 2-wire line. It holds all functions necessary for the easy creation of a HomePlug AV compatible network device.

The host interface can be configured to operate in two alternative modes:

- **PHY-Mode**
  Serves as a MII/RGMII PHY interface for connection to Ethernet MAC controllers.
- **Host-MODE**
  Serves as an MII/RGMII host interface for connection to an Ethernet PHY.

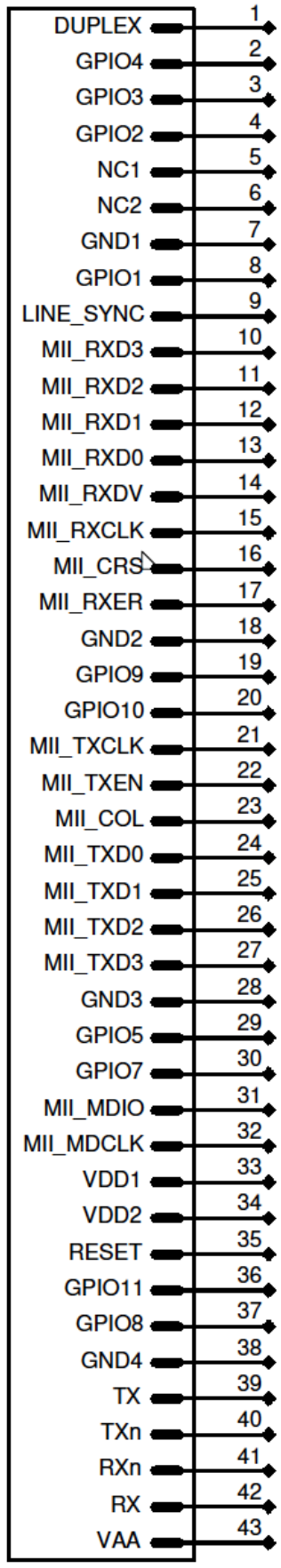
2.1. Features

- Supports up to 500 Mbps PHY rates over power line
- up to 300 m range via power cable (preliminary)
- up to 400 m range via telephone cable (prelim.)
- IEEE 1901 compatible HomePlugAV power line networking controller with MII/RGMII (MAC or PHY mode) interfaces
- Open API for status information and device configuration
- 128 bit AES link encryption with key management for enhanced security
- Simplifies development cycle, assembly, and testing
- AR7400 (AR7410) / AR1500 chipset
- Physical dimension: 27.5 mm x 69.5 mm
- Horizontal and vertical mounting version with straight and right-angle connector, respectively
- Cost-optimized design
- Designed for small-footprint embedded applications

2.1. Applications

- Ethernet extension via any wire
- Polarity agnostic 2-wire installation
- Retrofitting using existing wiring
- Ethernet anywhere
- Security Cameras
- AV-Intercoms
- Home Automation
- Voice-over-IP (VoIP)
- Audio and video streaming
- video distribution
- High speed broadband sharing

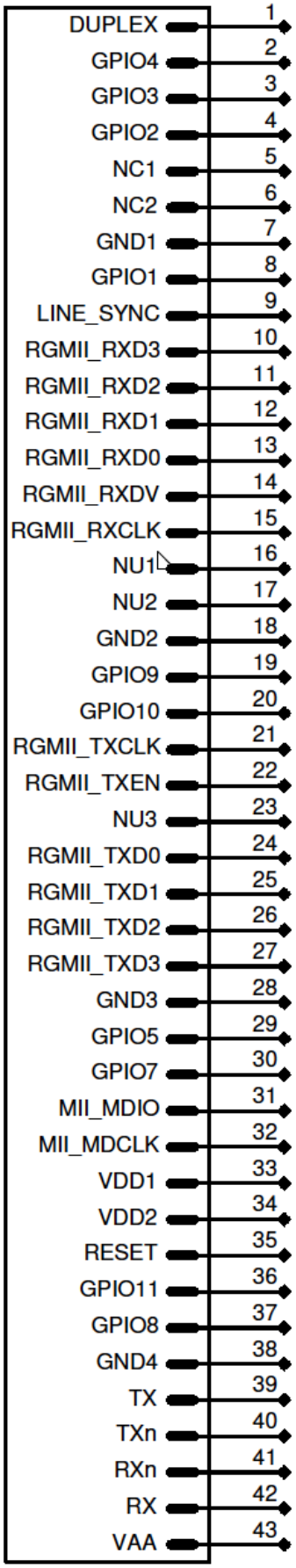
3. Pin-Assignment MII-Version (Fast-Ethernet)



Pin-#	Pin Name	Function
1	DUPLEX	strapping: Duplex Mode
2	GPIO4	strapping: SPEED_SEL[0]
3	GPIO3	strapping: ISODEF
4	GPIO2	strapping: ANEN
5	NC1	not connected, core voltage internally generated
6	NC2	not connected, core voltage internally generated
7	GND1	Ground
8	GPIO1	strapping: ENET_SEL[1] / Security Push Button
9	LINE_SYNC	AC line zero-cross detect signal
10	MII_RXD3	MII Receive Data Bit 3
11	MII_RXD2	MII Receive Data Bit 2
12	MII_RXD1	MII Receive Data Bit 1
13	MII_RXD0	MII Receive Data Bit 0
14	MII_RXDV	MII Receive Data Valid
15	MII_RXCLK	MII Receive Clock
16	MII_CRS	MII Carrier Sense
17	MII_RXER	MII Receive Error
18	GND2	Ground
19	GPIO9	strapping: DDR_SEL / LED: Ethernet Link
20	GPIO10	strapping: BM_SEL / LED: Powerline Mode
21	MII_TXCLK	MII Transmit Clock
22	MII_TXEN	MII Transmit Enable
23	MII_COL	MII Collision Detect
24	MII_TXD0	MII Transmit Data Bit 0
25	MII_TXD1	MII Transmit Data Bit 1
26	MII_TXD2	MII Transmit Data Bit 2
27	MII_TXD3	MII Transmit Data Bit 3
28	GND3	Ground
29	GPIO5	strapping: MD_A[3]
30	GPIO7	strapping: MD_A[4]
31	PHY_MDIO	MII management data I/O
32	PHY_MDCLK	MII management data clock
33	VDD1	+3.3V
34	VDD2	+3.3V
35	RESET	reset all module logic when low
36	GPIO11	strapping: SPEED_SEL[1] / LED: Power
37	GPIO8	strapping: MP_SEL / LED: Powerline Link
38	GND4	Ground
39	TX	Analog transmit+ output to transformer
40	TXn	Analog transmit- output to transformer
41	RXn	Analog receive- input from transformer
42	RX	Analog receive+ input from transformer
43	VAA	+11.2 V

Table 3.1: Pin Assignment MII-Version

4. Pin-Assignment RGMII-Version (Gigabit-Ethernet)



Pin-#	Pin Name	Function
1	DUPLEX	strapping: Duplex Mode
2	GPIO4	strapping: SPEED_SEL[0]
3	GPIO3	strapping: ISODEF
4	GPIO2	strapping: ANEN
5	NC1	not connected, core voltage internally generated
6	NC2	not connected, core voltage internally generated
7	GND1	Ground
8	GPIO1	strapping: ENET_SEL[1] / Security Push Button
9	LINE_SYNC	AC line zero-cross detect signal
10	RGMII_RXD3	RGMII Receive Data Bit 3
11	RGMII_RXD2	RGMII Receive Data Bit 2
12	RGMII_RXD1	RGMII Receive Data Bit 1
13	RGMII_RXD0	RGMII Receive Data Bit 0
14	RGMII_RXDV	RGMII Receive Data Valid
15	RGMII_RXCLK	RGMII Receive Clock
16	NU1	not used
17	NU2	not used
18	GND2	Ground
19	GPIO9	strapping: DDR_SEL / LED: Ethernet Link
20	GPIO10	strapping: BM_SEL / LED: Powerline Mode
21	RGMII_TXCLK	RGMII Transmit Clock
22	RGMII_TXEN	RGMII Transmit Enable
23	NU3	not used
24	RGMII_TXD0	RG MII Transmit Data Bit 0
25	RGMII_TXD1	RGMII Transmit Data Bit 1
26	RGMII_TXD2	RGMII Transmit Data Bit 2
27	RGMII_TXD3	RGMII Transmit Data Bit 3
28	GND3	Ground
29	GPIO5	strapping: MD_A[3]
30	GPIO7	strapping: MD_A[4]
31	PHY_MDIO	MII management data I/O
32	PHY_MDCLK	MII management data clock
33	VDD1	+3.3V
34	VDD2	+3.3V
35	RESET	reset all module logic when low
36	GPIO11	strapping: SPEED_SEL[1] / LED: Power
37	GPIO8	strapping: MP_SEL / LED: Powerline Link
38	GND4	Ground
39	TX	Analog transmit+ output to transformer
40	TXn	Analog transmit- output to transformer
41	RXn	Analog receive- input from transformer
42	RX	Analog receive+ input from transformer
43	VAA	+11.2 V

Table 4.1: Pin Assignment RGMII-Version

5. Detailed Pin Description by Group

5.1. Ethernet-Interface

Pin	MODE		Pin Name MII	Pin Name RGMII	Description
	MAC	PHY			
10 11 12 13	**I**	**O**	MII_RXD3 MII_RXD2 MII_RXD1 MII_RXD0	RGMII_RXD3 RGMII_RXD2 RGMII_RXD1 RGMII_RXD0	Ethernet Receive Data: The PHY controller drives RXD[3:0] and the MAC core receives RXD[3:0]. RXD[3:0] transition synchronously with respect to RXCLK. For each RXCLK period in which RXDV is asserted, RXD[3:0] is valid. RXD0 is the least-significant bit. The PHY controller tri-states RXD[3:0] in isolate mode.
14	**I**	**O**	MII_RXDV	RGMII_RXDV	Ethernet Receive Data Valid. The PHY controller asserts RXDV to indicate to the MAC core that it is presenting the recovered and decoded data bits on RXD[3:0] and that the data on RXD[3:0] is synchronous to RXCLK. RXDV transitions synchronously with respect to RXCLK. RXDV remains asserted continuously from the first recovered nibble of the frame through the final recovered nibble, and is de-asserted prior to the first RXCLK that follows the final nibble. The PHY controller tri-states MRX_DV in isolate mode.
15	**I**	**O**	MII_RXCLK	RGMII_RXCLK	Ethernet Receive Clock. RXCLK is a continuous clock that provides the timing reference for the transfer of the RXDV and RXD[3:0] signals from the PHY controller to the MAC core. The PHY controller always sources RXCLK. RXCLK frequency is equal to 25% of the data rate of the received signal on the Ethernet cable in MII 10/100 Mbps mode, and 12.5% of the data rate of the received signal on the Ethernet cable in RGMII 1000 Mbps mode. The PHY controller tri-states RXCLK in isolate mode.
16	**I**	**O**	MII_CRS	NU1	MII Ethernet Carrier Sense - MII only, not used in RGMII: The PHY controller asserts CRS when either transmit or receive medium is non-idle. The PHY de-asserts CRS when both transmit and receive medium are idle. The PHY must ensure that CRS remains asserted throughout the duration of a collision condition. The transitions on the CRS signal are not synchronous to either the TXCLK or the RXCLK. The PHY controller tri-states CRS in isolate mode.
17	**I**	**O**	MII_RXER	NU2	MII Ethernet Receive Error - MII only, not used in RGMII: The PHY controller asserts RXER high for one or more RXCLK periods to indicate to the MAC core that an error (a coding error or any error that the PHY is capable of detecting that is otherwise undetectable by the MAC) was detected somewhere in the current frame. RXER transitions synchronously with respect to MRXCLK. While RXDV is de-asserted, RXER has no effect on the MAC core. The PHY controller tri-states RXERR in isolate mode.
21	**I**	**O**	MII_TXCLK	/	Ethernet Transmit Clock: TXCLK is a continuous clock that provides a timing reference for the transfer of the TXEN and TXD[3:0] signals from the MAC core to the PHY controller. The PHY controller supplies TXCLK in 10/100 Mbps MII mode. The operating frequency of TXCLK is 25 MHz when operating at 100 Mbps and 2.5 MHz when operating at 10 Mbps. The PHY controller tri-states TXCLK in isolate mode.
21	**O**	**I**	/	RGMII_TXCLK	Ethernet Transmit Clock: TXCLK is a continuous clock that provides a timing reference for the transfer of the TXEN and TXD[3:0] signals from the MAC core to the PHY controller. The operating frequency of TXCLK is 125 MHz when operating at 1000 Mbps, 25 MHz when operating at 100 Mbps and 2.5 MHz when operating at 10 Mbps. The PHY controller ignores TXCLK in isolate mode.
22	**O**	**I**	MII_TXEN	RGMII_TXEN	Ethernet Transmit Enable. A high assertion on TXEN indicates that the MAC core is presenting nibbles to the PHY controller for transmission. The AR7400 MAC core asserts TXEN with the first nibble of the preamble and keeps TXEN asserted while all nibbles to be transmitted are presented to the MII. TXEN is de-asserted prior to the first TXCLK following the final nibble of the frame. TXEN transitions synchronously with respect to TXCLK. The PHY controller ignores TXEN in isolate mode.
23	**I**	**O**	MII_COL	NU3	MII Ethernet Collision Detected - MII only, not used in RGMII: The PHY controller asserts COL when it detects a collision on the medium. COL remains asserted while the collision condition persists. COL signal transitions are not synchronous to either the TXCLK or the RXCLK. The MAC core ignores the COL signal when operating in the full-duplex mode. The PHY controller tri-states COL in isolate mode

24 25 26 27	**O**	**I**	MII_TXD0 MII_TXD1 MII_TXD2 MII_TXD3	RGMII_TXD0 RGMII_TXD1 RGMII_TXD2 RGMII_TXD3	Ethernet Transmit Data: The MAC core drives TXD[3:0] and the PHY controller receives TXD[3:0]. TXD[3:0] transition synchronously with respect to TXCLK. For each TXCLK period in which TXEN is asserted, TXD[3:0] is valid. TXD0 is the least-significant bit. The PHY controller ignores TXD[3:0] in isolate mode.
31	**I/O**	**I/O**	PHY_MDIO	PHY_MDIO	PHY Management Data In/Out. This is the control data input signal from the PHY controller. The PHY drives the Read Data synchronously with respect to the MDCLK clock during the read cycles. This is also the control data output signal from the MAC core that drives the control information during the Read/Write cycles to the PHY controller. The MAC core drives the MDIO signal synchronously with respect to the MDCLK.
32	**O**	**I**	PHY_MDCLK	PHY_MDCLK	PHY Management Data Clock: The MAC core sources MDCLK as the timing reference for transfer of information on the MDIO signals. MDCLK signal has no maximum high or low times. MDCLK minimum high and low times are 160 ns each, and the minimum period for MDCLK is 400 ns.

Table 5.1: Ethernet Signals

5.2. GPIO-Pins - Strap Options

There are a total of 11 General Purpose I/O-Pins, which have dual functions: They serve as pin-strapping and are sampled during reset in order to select different operation modes. During normal operation these pins are used to drive LED outputs or to connect a push-button. The functions of the pins is different for the MAC-Mode and the PHY-Mode. Please refer to section 6 for a detailed description of these functions.

Pin	Internal Pull-Up/Down	Pin Name	Function	Description
1	Pull-Up	DUPLEX	Duplex Mode	Strap = 1: Full-Duplex (Default) Strap = 0: Half-Duplex
8	version dependent	GPIO1	ENET_SEL[1]	Strap = 1: MII 10/100 Operation (Default on 2LAN500-xC) Strap = 0: RGMII 10/100/1000 Operation (Default on 2LAN500-xI)
4	Pull-Up	GPIO2	ANEN	Strap = 1: Auto-negotiate enabled (Default) Strap = 0: Auto negotiate disabled
3	Pull-Down	GPIO3	ISODEF	Strap = 1: MII/RGMII interface is isolated Strap = 0: MII/RGMII interface is active (Default)
2	Pull-Up	GPIO4	SPEED_SEL[0]	SPEED_SEL[1:0] - Ethernet Speed 00 = 10 Mbps 01 = 100 Mbps (Default) 10 = 1000 Mbps 11 = Reserved
36	Pull-Down	GPIO11	SPEED_SEL[1]	
29	Pull-Up	GPIO5	MD_A[3]	MD_A[4:3] - PHY Management Address 00 = 0x00 01 = 0x08 (Default) 10 = 0x10 11 = 0x18
30	Pull-Down	GPIO7	MD_A[4]	
37	Pull-Up	GPIO8	MP_SEL	Strap = 1: MAC-Mode (Default) Strap = 0: PHY-Mode
19	Pull-Up	GPIO9	DDR_SEL	Only DDR_SEL=1, do not use external pull-down! External memory is always DDR1.
20	Pull-Up	GPIO10	BM_SEL	Only BM_SEL=1, do not use external pull-down! Always boot from SPI-flash on module.

Table 5.2: GPIO Signals for pin strapping

5.3. Special Function Pins

Pin	MODE MAC	MODE PHY	Pin Name	Description
9	I	I	LINE_SYNC	Zero Cross Detector Input. This signal is connected to an external zero cross detector that provides a logic level signal with safety isolation from the AC power line waveform. This signal informs the AR7400 of the power line frequency and timing.
35	I/O	I/O	RESET	The reset for all logic is internally generated by the DC/DC converter for the core voltage: The regulator has a power-good open drain output, which is delayed app. 215ms from the time the power-good signal is issued. Alternatively an external reset signal may be supplied to this open drain output but is not required. The external signal needs to be driven low for at least 100ms after all supply voltages are stable.

Table 5.3: Special Function Signals

5.4. Line Interface

For compatibility reasons, TX, RX and TXn, RXn are connected to 4 different pins, although these signals are internally connected, respectively. The older INT6400 based designs used a 4-wire analog interface, requiring 2 separate primary windings of the transformer. The AR7400/AR1500 based design uses a single primary winding for transmit as well as receive. See section 7 for the transformer interface.

Pin	MODE MAC	MODE PHY	Pin Name	Description
39	O	O	TX	Analog Transmit Output, internally connected to RX = TXRX+
40	O	O	TXn	Analog Transmit Output (complementary), internally connected to RXn = TXRX-
41	I	I	RXn	Analog Receive Input (complementary), internally connected to TXn = TXRX-
42	I	I	RX	Analog Receive Input internally, connected to TX = TXRX+

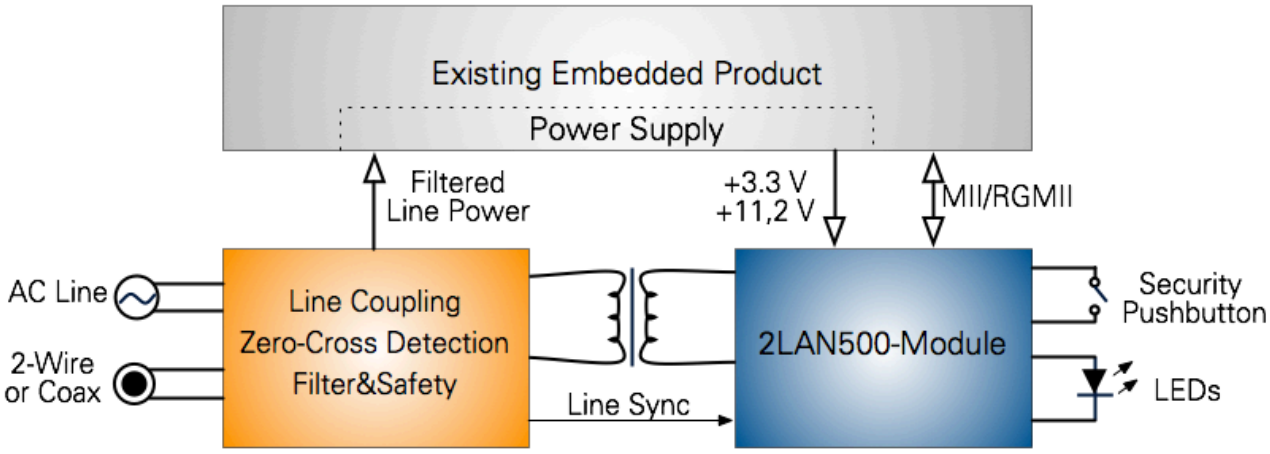
Table 5.4: AFE Line Interface Signals

5.5. Power

Pin	MODE MAC	MODE PHY	Pin Name	Description
7 18 28 38	I	I	GND	Ground Reference
33 34	I	I	VDD	+3.3V digital power
43	I	I	VAA	+11.2V analog power
5 6	/	/	NC	Not internally connected: For compatibility to the devolo dLAN200 module, which used these pins for the core power supply, these pins remain unused. The 2LAN500 module generates the core voltage internally from the +3.3V supply.

Table 5.5: Power Signals

6. Configuration of the 2LAN500 Module



In order to integrate the 2LAN500 module into an embedded design, the customer needs to provide the following interfaces, external to the module:

- Power supply: +3.3 V and +11.2 V - see section 8.1 for power requirements
- AC-Line coupling (or telephone wire / coax coupling) and zero-cross detection including filters and safety components - see section 7 for an application example.
- MII/RGMII Ethernet interface
- Optionally connection of status LEDs and a security pushbutton

In the following all configuration and signal options are described.

6.1. Host Interface Mode Selection

The host interface for the 2LAN500 module can be configured to one of the following two modes:

- **MII/RGMII PHY mode:** In this mode the module behaves like an Ethernet PHY using an MII/RGMII interface. The module can be configured as an Ethernet PHY to replace an existing Ethernet PHY on a developed product. In this mode, configuration and status information is available using the IEEE 802.3 MDI interface.

- **MII/RGMII MAC mode:** In this mode the module behaves like an Ethernet host device using an MII/RGMII interface. The module can be configured in MAC mode to connect to any other device that behaves like an Ethernet PHY. In the MAC mode, configuration and status information is available using the IEEE 802.3 MDI interface.

Host mode is selected through the use of the **HM_SEL** strapping at **GPIO 8**. The default mode without any external straps is MAC mode (1).

HM_SEL	Mode	Possible Application
0	PHY	• Alternative PHY for power line communication • Alternative PHY for 2Wire transmission
1 (Default)	MAC	• Ethernet to HomePlug Adapter • Connect to devices without MII-interface using PHY-to-PHY connection

Table 6.1: Host Interface Mode Selection

6.2. Ethernet Configuration (PHY Mode only)

If the Host Interface Mode is configured for PHY mode, there are additional configuration straps that are unique to the Ethernet PHY mode of operation shown in Table 6.2. The table also states the required pin strappings for MAC mode.

SPEED_SEL[1:0] select sets the MII/RGMII data rate. With internal straps the data rate defaults to 100 Mbps. Only when a data rate of 10 Mbps is required, SPEED_SEL0 needs to be strapped to '0'. In almost all cases no pin strapping should be required.

For versions with RGMII interface the data rate has been set to 1000 Mbps, so no pin strapping is required as well.

Auto-negotiation (ANEN) enables auto-negotiation of the parameters for speed and duplex mode or defaults the Ethernet interface to the preset speed and duplex settings.

DUPLEX selects the transmission mode for the MII interface, either in full-duplex (default) or half-duplex mode. The RGMII interface always operates in full-duplex mode.

ISODEF controls whether MII/RGMII signals are active or tri-stated.

Signal Name	Pin Name	MAC Mode	PHY Mode
SPEED_SEL1 **SPEED_SEL0**	GPIO11 GPIO4	0 or 1 don't care	SPEED_SEL[1:0] - Ethernet speed **00** = 10 Mbps **01** = 100 Mbps (Default) **10** = 1000 Mbps **11** = Reserved
MD_A4 **MD_A3**	GPIO7 GPIO5	0 or 1 don't care	MD_A[4:3] - PHY Management Address **00** = 0x00 **01** = 0x08 (Default) **10** = 0x10 **11** = 0x18
ANEN	GPIO2	0 or 1 don't care	**1** = Auto-negotiate enabled (Default) **0** = Auto negotiate disabled
DUPLEX	DUPLEX	NC do not connect	**1** = Full-Duplex (Default) **0** = Half-Duplex (only supported on MII interface)
ISODEF	GPIO3	**0**	**1** = Interface isolated **0** = Active Interface (Default)

Table 6.2: Ethernet Configuration Straps

6.3. LED-Indicators

The 2LAN500 module offers the connection of LED status indicators. The pins for the LEDs are GPIO pins, which serve the double purpose of pin strapping for mode configuration AND LED indicators. Depending on the polarity of the pin strapping, the LEDs have to be connected in one of the 2 following ways:

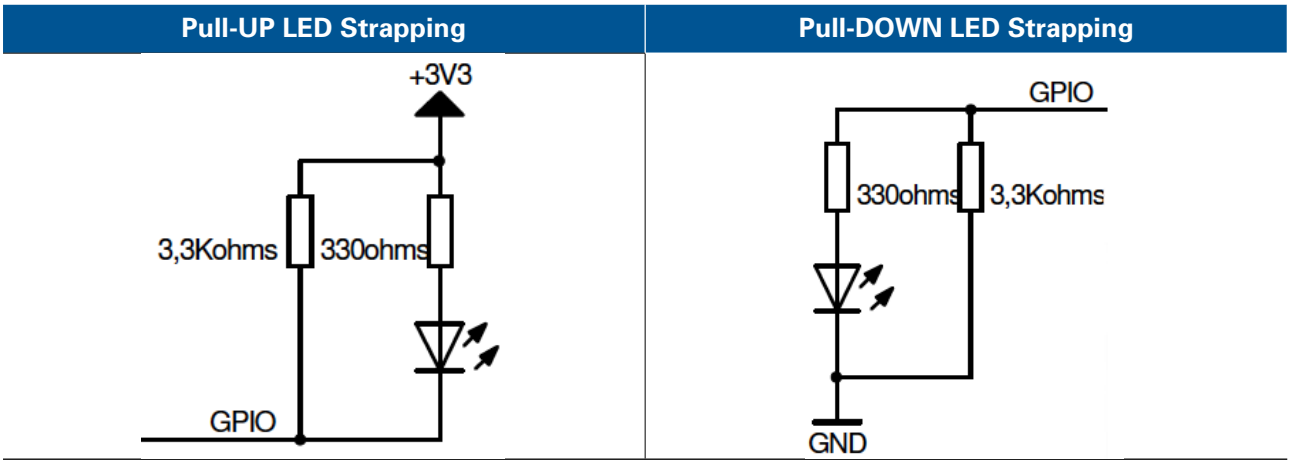


Fig. 6.3: Connection of LED Indicators

Component values in the figures above are typical. The value of the current limiting resistor is selected based on the desired LED current. Note that the maximum LED current must be limited to 12 mA.

The system status LEDs are controlled by routines in the MAC firmware. The status LED indicator configuration is listed in Table 6.3. Any two signals can also be connected to dual color LEDs.

Status LED	Pin Name	LED States		
		ON	FLASH	OFF
Power	GPIO11	Ready	Loading Firmware	Not Ready
Host/Ethernet Link	GPIO9	Ethernet Link Detected	Transmit or Receive Activity	No Link Detected
Powerline Mode	GPIO10	HomePlug 1.0 Traffic Detected	N/A	Silence
Powerline Link	GPIO8	Powerline Link Detected	Powerline Activity Detected	No Powerline Link Detected

Table 6.3: LED Status Indicators

6.4. Security Pushbutton

The security pushbutton provides an easy method for pairing two or more dLAN devices. By pressing the pushbutton for a short period of time on each device that should be added to the network the devices are connected as if they had the same password.

The Security Pushbutton is connected to **GPIO1**. The strapping of this pin - UP or DOWN - depends on the 2LAN500 version: The RGMII-version (i.e. the industrial temp. version) requires the GPIO1 pin to be strapped DOWN. Conversely, the MII-version (i.e. the commercial temp. version) requires the GPIO1 pin to be strapped UP. Therefore are are 2 different schematics for the security pushbutton:

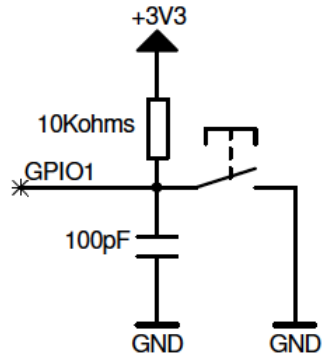
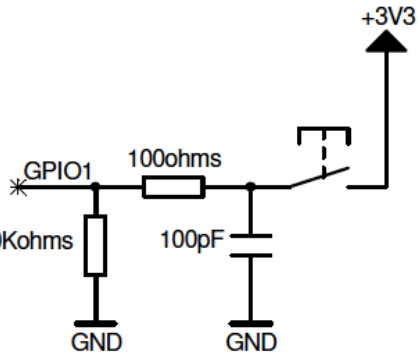
Security Pushbutton for Pull-UP MII interface / C-Temp version	Security Pushbutton for Pull-DOWN RGMII interface / I-Temp version
	

Fig. 6.4: Connection of Security Pushbutton

7. Application Example

7.1. Powerline Interface with RGMII version, PHY mode

Figure 7.1 gives an application example of how to connect the 2LAN500 module for PHY mode applications. In contrast to INT6400 based designs, no external over-voltage protection on the TX/RX-lines is required: All protection has been integrated in the module.

The AC zero cross detector is based on an opto-isolator to provide the required safety isolation between the power line and the low voltage secondary circuitry. The LED of the opto-isolator is connected to the power line in series with two high value resistors. The resistors limit the current (and voltage) that can flow through the LED during both forward conduction (ON state) and reverse bias (OFF state). The emitter of the phototransistor connects to low voltage ground. A pull-up on the collector side is provided on the module.

The high capacitances of the LED and phototransistor result in a relatively slow response time. The slow response provides low pass filtering which greatly reduces timing shift from noise or OFDM signals on the powerline.

Coupling capacitors and the secondary of the coupling transformer form a high-pass filter that allows the Powerline communications signal to pass, but blocks 50/60Hz AC sine wave. The resistors parallel to the capacitors serve to discharge the coupling capacitors when the device is removed from the AC line.

Transient protection is accomplished through a Metal Oxide Varistor. (MOV). For 230Vac networks at least a 300Vac MOV should be used. However, the MOV also presents an across-the-line capacitance of 100 pF or more. This capacitance can severely reduce the receive signal level at the upper (high frequency) end of the AR7400 communication band. Placing the MOV behind high frequency (high quality) inductors isolates this shunt capacitance. These inductors provide the added benefit of further isolating noise generated by the switching power supply from the communication signal path. The 220 Ω resistor in parallel with the inductors lowers the inductor Q and minimizes self resonance of the inductor. A frequency dependent variable impedance shunt component in the PLC front end circuit would reduce data rate performance by making the front end impedance frequency dependent.

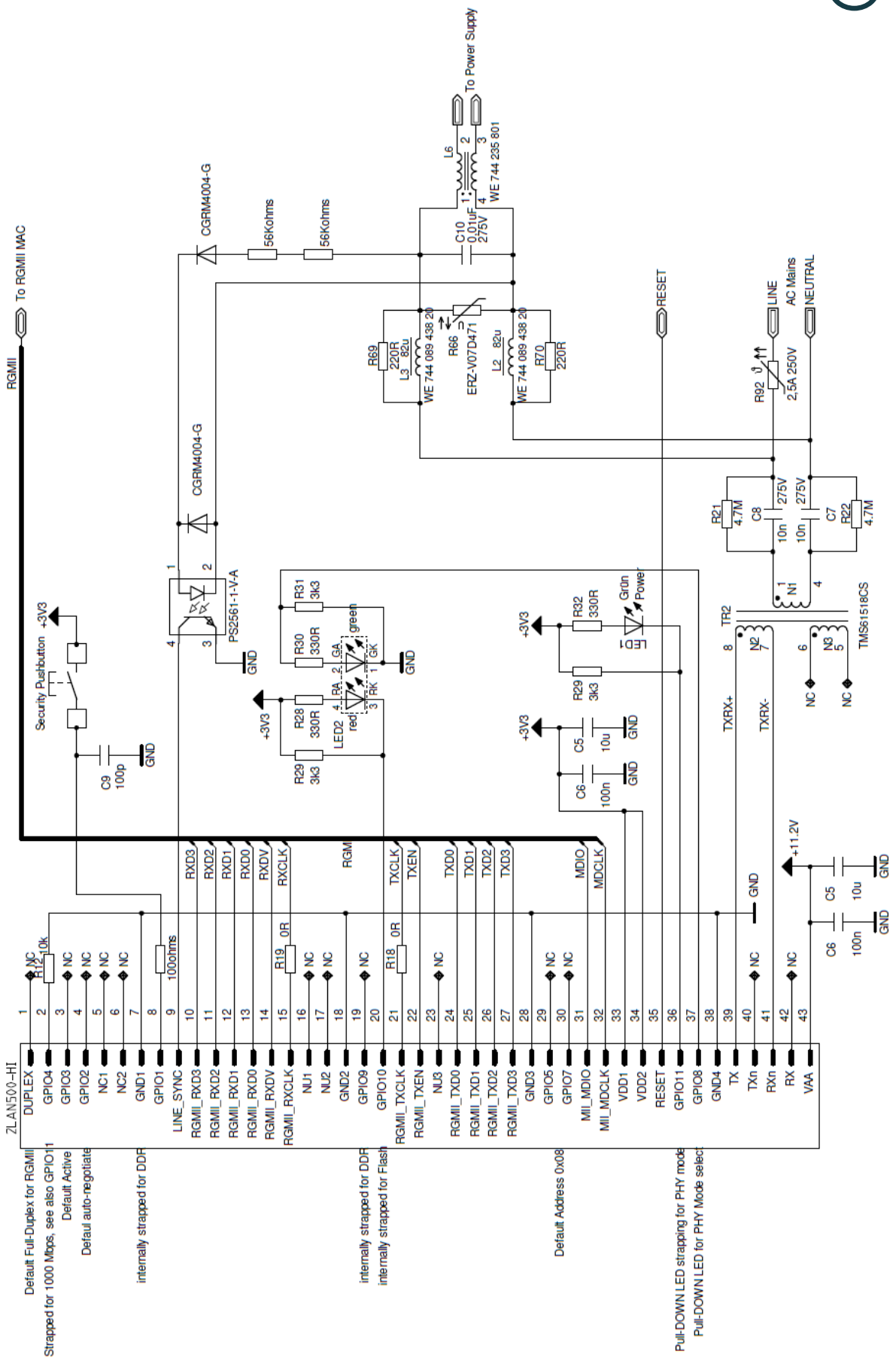


Fig. 7.1: 2LAN500 RGMII schematic for PHY mode

7.2. 2-Wire/telephone cable interface with MII version, MAC mode

If powerline communication i.e. transmission via AC-mains is not required and the signals are instead transmitted via a telephone or bell wire, the schematic of Fig. 7.1 can be simplified as the zero-cross detector can be omitted. For compatibility with existing INT6400 based designs, the wiring of the PLC-signals to a transformer with 2 primary windings is shown. For new designs the transformer in the appendix is recommended.

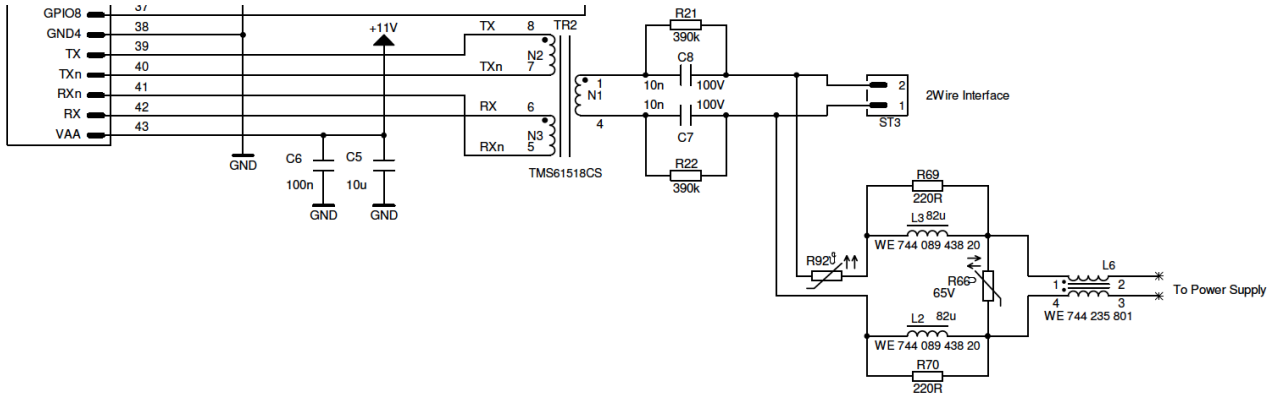


Fig. 7.2a: 2LAN500 MII line coupler for telephone or bell wire line

As in the schematic depicted in figure 7.1 it is likewise important for the low-voltage telephone wire design to isolate the capacitance of the Metal Oxide Varistor (MOV) from the PLC line.

- MOV surge suppression component capacitance is isolated by special high frequency inductors L2 and L3
- High impedance inductive isolation in front end and the common mode choke eliminate power supply switching noise and low impedance from interfering with the PLC signal

The followingFigure 7.2b shows the complete schematic (without power supply).

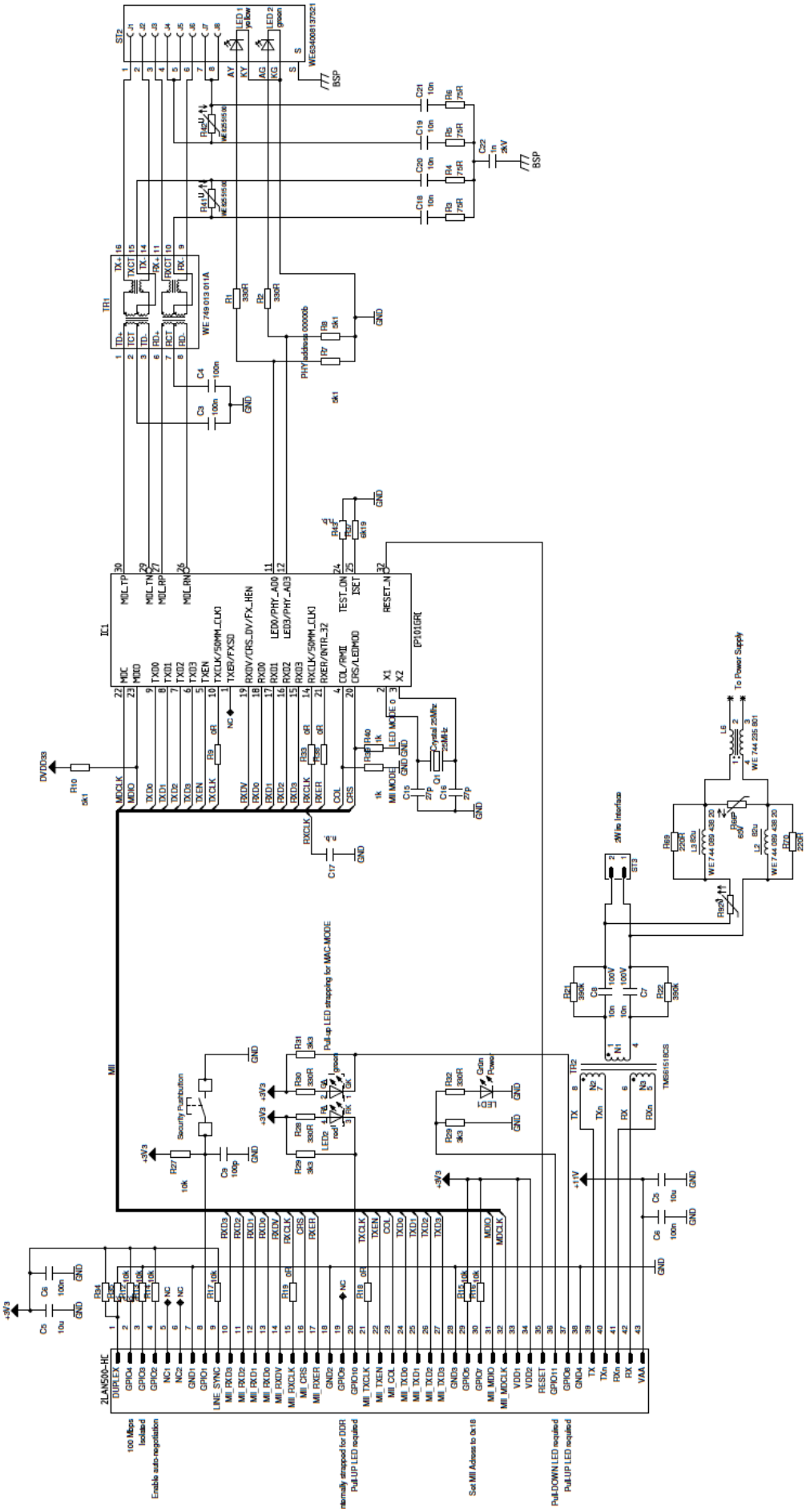


Fig. 7.2b: 2LAN500 MII schematic for MAC mode including 10/100 PHY and Ethernet interface

7.3. RGMII Ethernet interface

The AR7400 supports both MAC mode and PHY mode Ethernet interfaces. In MAC mode the AR7400 connects to an external Ethernet transceiver (PHY). The AR7400 uses RGMII to connect to the PHY and supports 10BaseT, 100BaseTX, and 1000BaseT. The PHY IC can be any standard IC as long as it satisfies requirements specified in the AR7400 data sheet. The current reference application uses Atheros' AR8035.

Because of the speed at which RGMII functions when at 1 gigabit rate, there are special requirements for the routing of these signal traces such as trace impedance, spacing, and electrical length. There are two different match groups. Within each match group, the maximum trace length should be less than 50 mm and the electrical length must match within 5%. This is critical. The two match groups are:

Group 1	Group 2
RGMII_TXCLK	RGMII_RXCLK
RGMII_TXEN	RGMII_RXDV
RGMII_TXD[3:0]	RGMII_RXD[3_0]

Table 7.3: RGMII Match Groups

The 2LAN500 Module supports RGMII v1.3 with internal delay. Automatically 2 ns nominal delay is added on the RGMII_TXCLK signal.

8. 2LAN500 Specifications

8.1. Power Supply Requirements

The 2LAN500 module needs 3.3 V and 11.2 V for operation. The typical power consumption is app. 2 W. The core voltage of 1.05 V and the DDR voltage of +2.5 V are generated internally from the 3.3 V supply.

The applied VAA voltage MUST be set to a range of no less than 11 V to a MAXIMUM of 11.4 V. A precision LDO regulator is recommended.

Symbol	Min	Typ	Max
VDD Supply Voltage	3.13 V	3.30 V	3.47 V
VDD Supply Current	200 mA	300 mA	400 mA
VAA Supply Voltage	11.0 V	11.2 V	11.4 V
VAA Supply Current	70 mA	80 mA	90 mA

Table 8.1: Power Supply Requirements

8.2. Absolute Maximum Ratings

Operation at or above the absolute maximum ratings may cause permanent damage to the device. Exposure to these conditions for extended periods of time may affect long-term device reliability. Correct functional behavior is not implied or guaranteed when operating at or above the absolute maximum ratings.

The analog power supply voltage (VAA) should not be applied without the 3.3 V (VDD) power supply voltage! Otherwise, there are no special requirements with regards to power sequencing.

Symbol	Parameter	Min	Max
VDD	Power Supply Voltage	-0.3 V	3.6 V
VAA	Analog Voltage	-0.3 V	12.5 V
T_{STORE}	Storage Temperature	-40 °C	+150 °C
$T_{OPERATE}$	Operation Temperature Commercial Temp. Version	0 °C	+60 °C
$T_{OPERATE}$	Operation Temperature Industrial Temp. Version	-40 °C	+85 °C
V_{ESD}	Human Body Model	–	2 kV

Table 8.2: Absolute Maximum Ratings

8.3. DC Characteristics

Symbol	Parameter	Test Conditions	Min	Max
V_{IL}	Low-Level input voltage		–	0.8 V
VIH	High-Level input voltage		2.0 V	–
VOL	Low-Level output voltage	IOL = 4 mA all other interfaces IOL = 12 mA for GPIOs		0.4 V
VOH	High-Level output voltage	IOL = -4 mA all other interfaces IOL = -12 mA for GPIOs	2.4 V	–
IIL	Low-Level input current	VI = GND	-1 µA	–
IIH	High-Level input current	VI = VDD	–	+1 µA
IOZ	High-impedance output current	GND ≤ VI ≤ VDD	-1 µA	+1 µA

Table 8.3: DC Characteristics

8.4. PCB Layout Top- / Bottom-Layer

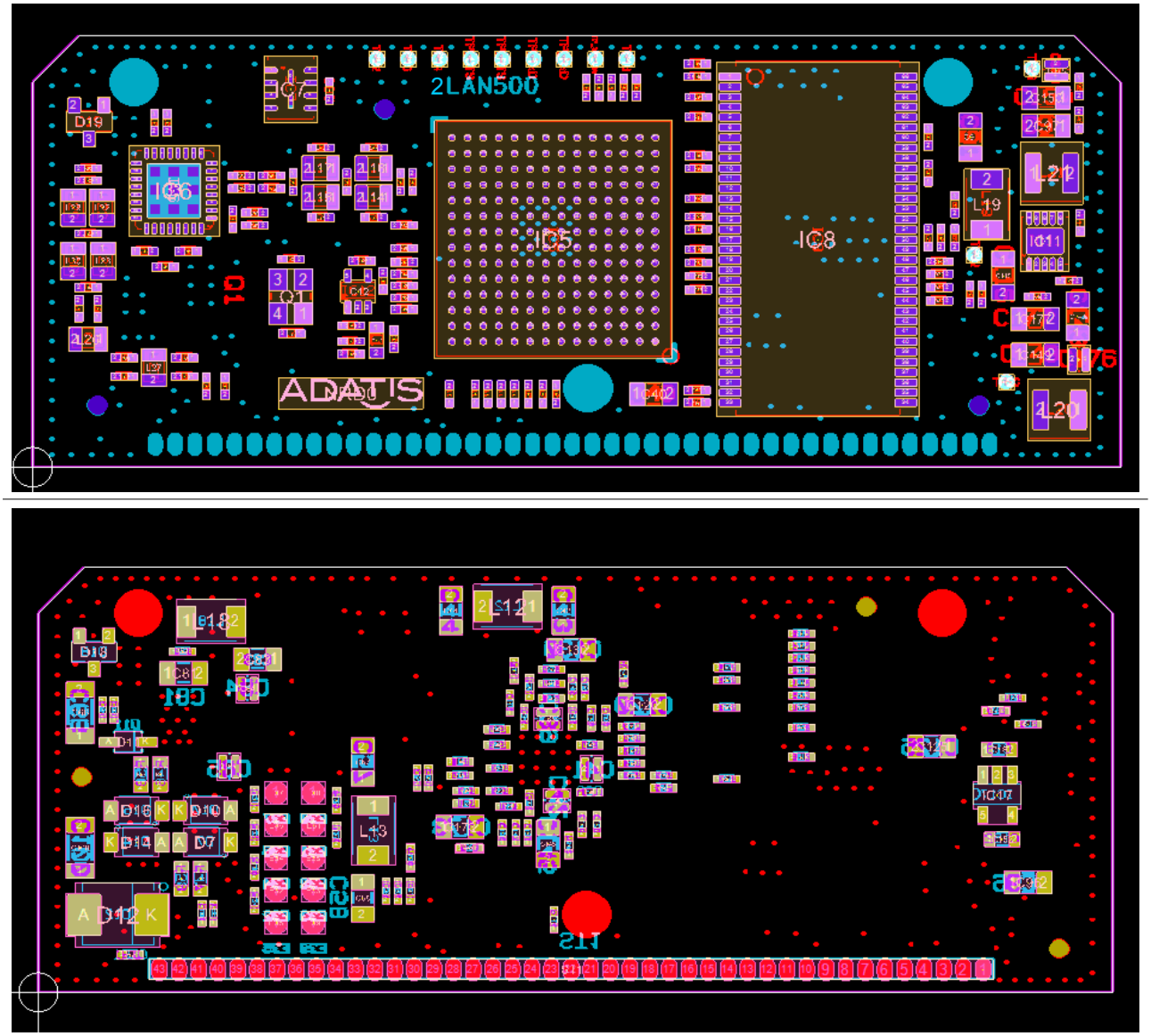


Figure 8.4: Top and Bottom Component Placement

8.5. Mechanical Specifications

The 2LAN500 module is connected via an industry standard 43-pin header using 0.46 mm square pins on 0.127 mm (half pitch) centers. For easy insertion and removal of module devices a mating female connector can be used. Alternatively, the device may be soldered directly to the host board.

Connectors used:

- Vertical version: Samtec: TMS-143-02-L-S-RA (Lead Size: (0.46 mm) .018" SQ)
- Horizontal version: Samtec: FTS-143-01-F-S (Lead Size: (0.41 mm) .016“ SQ)

The card dimensions including connector are:

- Vertical version: 69.55 x 32.64 x 8.8 mm
- Horizontal version: 69.5 x 27.5 x 13.8 mm

The design has been driven by compatibility to the devolo dLAN200 board. Therefore the shape and size of the PCB, the type and location of the connector and the 3 mounting holes have been kept compatible.

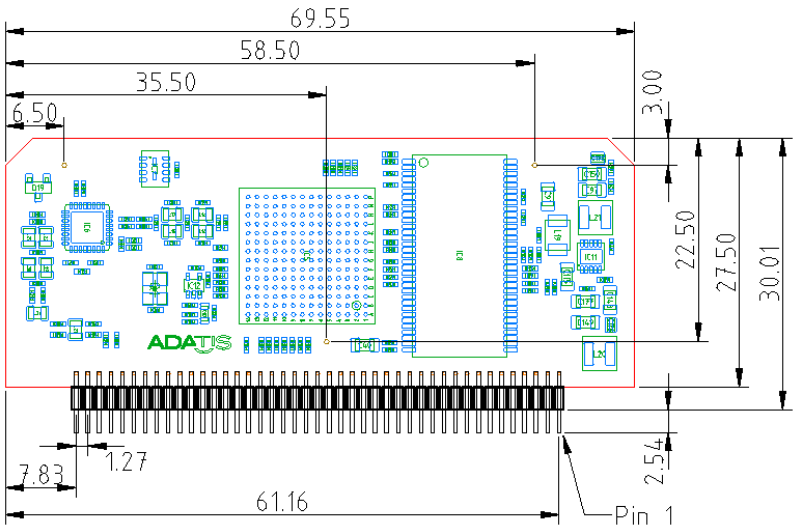
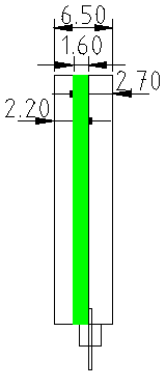
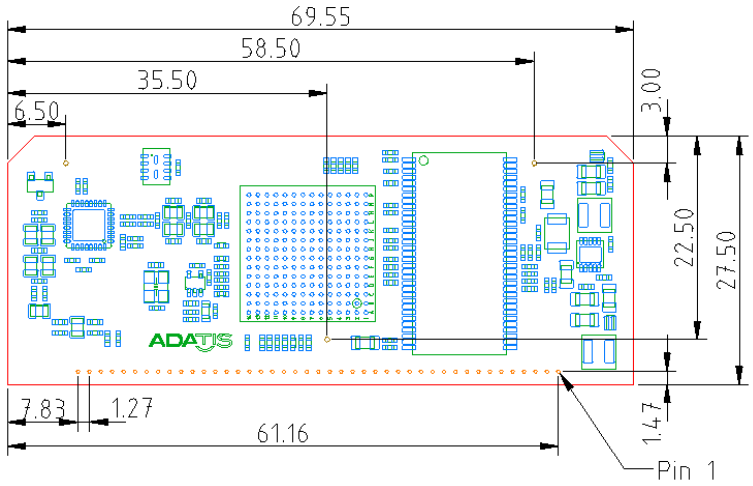
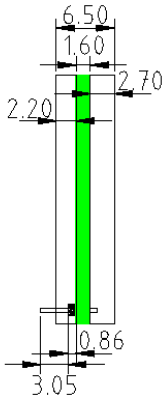
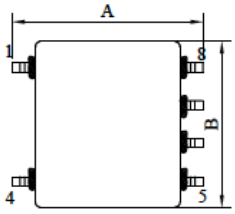
Version	Top-View	Side-View
2LAN500-Vx		
2LAN500-Hx		

Table 8.5: Mechanical Specifications

9. Appendix

9.1. Transformer Data Sheet

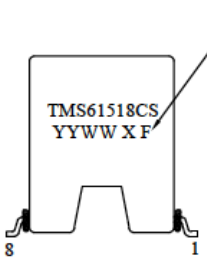
1. DIMENSIONS(UNIT:mm)



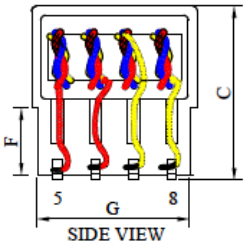
TOP VIEW

A: 12.5 ±0.5
B: 10.9 ±0.2
C: 11.5MAX
D: 2.5 ±0.3
E: 7.5 ±0.5
F: 4.4 ±0.2
G: 9.9 ±0.2

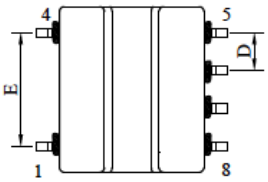
Marking:
YY: Year
WW: Week
X:Means as below content
A----Monday
B----Tuesday
C----Wednesday
D----Thursday
E----Friday
F----Saturday
G----Sunday



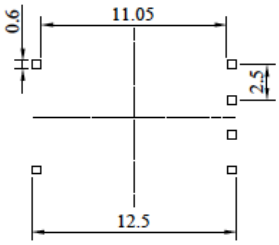
FRONT VIEW



SIDE VIEW

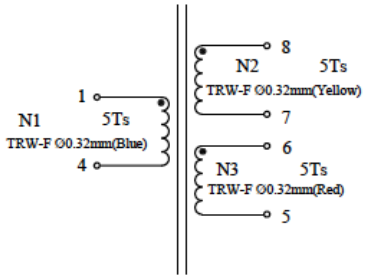


BOTTOM VIEW



PINS LAYOUT

2. SCHEMATIC:



• Mean start winding

3.ELECTRICAL CHARACTERISTIC: At 25°C

a).INDUCTANCE: @1KHz,1V
L(1-4): 10.9 uH +50%/-35%
L(8-7): 10.9 uH +50%/-35%
L(6-5): 10.9 uH +50%/-35%

b).DC RESISTANCE:
DCR(1-4): 30.0 mOhm MAX
DCR(8-7): 30.0 mOhm MAX
DCR(6-5): 30.0 mOhm MAX

c).HI-POT:
PINS 1,4, TO 6,5,8,7: 5mA MAX @3.0KVac, 60sec, 60Hz

4. CONSTRUCTIONS:

NO.	Winding	Terminal	Wire	Turns	Remark
1	N1	1 - 4	TRW-F Ø0.32mm(Blue)	5Ts	Parallel Winding
2	N2	8 - 7	TRW-F Ø0.32mm(Yellow)	5Ts	
3	N3	6 - 5	TRW-F Ø0.32mm(Red)	5Ts	

5.MATERIAL LIST

ITEM	DESCRIPTION	SUPPLIER	UL NO.
CORE	T9*5*3C TP5	TDG	N/A
WIRE	TRW-F Ø0.32mm(YELLOW)	GREAT LEOFLON	E211989
WIRE	TRW-F Ø0.32mm(BLUE)	GREAT LEOFLON	E211989
WIRE	TRW-F Ø0.32mm(RED)	GREAT LEOFLON	E211989
CASE	9.5*11*8.2 PM9630	SUMITOMO	E41429

6.NOTES:

Remove PIN2,3

Transtek Magnetics INC
Http://www.transtekmagnetics.com

DESCRIPTION: TRANSFORMER

RoHS COMPLIANT

TOLERANCE (UNLESS OTHERWISE SPECIFIED)	SCALE:	DRAWING NO.:	CUSTOMER:	
0<L<5:±0.1 5<L<16:±0.3 16<L<50:±0.5	NTS.	TR09090502	CUSTOMER P/N: 81752	REV.: --
ANGLE: ±1°		PAGE NO.: 2 OF 3	TRANSTEK P/N: TMS61518CS-1	REV.: F