BG95&BG96

Compatible Design

LPWA Module Series

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About the Document

Revision History

Revision	Date	Author	Description
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Contents

Table Index

Figure Index

1 Introduction

Quectel LTE Cat M1/Cat NB2/EGPRS module BG95 is compatible with Quectel LTE Cat M1/Cat NB1/EGPRS module BG96. This document briefly describes the compatible design between BG95 and BG96 modules.

2 General Descriptions

2.1. Product Description

BG96 is an embedded LPWA (LTE Cat M1/LTE Cat NB1/EGPRS) wireless communication module. It provides data connectivity on LTE-TDD/LTE-FDD/GPRS/EGPRS networks, and supports half-duplex operation in LTE networks. It also provides GNSS [1)] and voice [2)] functionality to meet customers' specific application demands. For more details, please refer to ***document [1]***.

BG95 is an embedded LPWA (LTE Cat M1/LTE Cat NB2 [3)]/EGPRS) wireless communication module. It provides data connectivity on LTE-FDD/GPRS/EGPRS networks, and supports half-duplex operation in LTE networks. It also provides GNSS and voice [2)] functionality to meet customers' specific application demands. BG95 includes seven variants: BG95-M1, BG95-M2, BG95-M3, BG95-N1, BG95-M4*, BG95-M5* and BG95-MF [4)]. For more details, please refer to ***document [2]***.

BG95 and BG96 are designed as compatible products. Customers can choose a suitable module according to specific application requirements. The compatible design guideline ensures a smooth migration between the modules for customers' products.

Table 1: Module General Information

Module	Appearance	Packaging	Dimensions (mm)	Description
BG96		102-pin LGA	26.5 × 22.5 ×2.3	LTE Cat M1/Cat NB1/ EGPRS module
BG95		102-pin LGA	23.6 × 19.9 × 2.2	LTE Cat M1/Cat NB2/ EGPRS module

Table 2: Frequency Bands and GNSS Types of BG95 and BG96 Modules

Module	Supported Bands	LTE Bands Power Class	GNSS [1)]
BG96	**Cat M1:** LTE-FDD: B1/B2/B3/B4/B5/B8/B12/B13/ B18/B19/B20/B25 [5)]/B26*/B28 LTE-TDD: B39 **Cat NB1:** LTE-FDD: B1/B2/B3/B4/B5/B8/B12/B13/ B18/B19/B20/B25 [5)]/B26*/B28 **EGPRS:** 850/900/1800/1900MHz	Power Class 3 (23dBm)	GPS, GLONASS, BeiDou/Compass, Galileo, QZSS
BG95-M1	**Cat M1 Only:** LTE-FDD: B1/B2/B3/B4/B5/B8/B12/B13/ B14/B18/B19/B20/B25/B26/B27/ B28/B66/B85	Power Class 5 (21dBm)	GPS, GLONASS, BeiDou/Compass, Galileo, QZSS
BG95-M2	**Cat M1:** LTE-FDD: B1/B2/B3/B4/B5/B8/B12/B13/ B14/B18/B19/B20/B25/B26/ B27/B28/B66/B85 **Cat NB2:** LTE-FDD: B1/B2/B3/B4/B5/B8/B12/B13/ B18/B19/B20/B25/B26/B28/B66/ B71/B85	Power Class 5 (21dBm)	GPS, GLONASS, BeiDou/Compass, Galileo, QZSS
BG95-M3	**Cat M1:** LTE-FDD: B1/B2/B3/B4/B5/B8/B12/B13/ B14/B18/B19/B20/B25/B26/B27/ B28/B66/B85 **Cat NB2:** LTE-FDD: B1/B2/B3/B4/B5/B8/B12/B13/ B18/B19/B20/B25/B26/ B28/B66/B71/B85 **EGPRS:** 850/900/1800/1900MHz	Power Class 5 (21dBm)	GPS, GLONASS, BeiDou/Compass, Galileo, QZSS
BG95-N1	**Cat NB2 Only:**	Power Class 5 (21dBm)	GPS,

	LTE FDD: B1/B2/B3/B4/B5/B8/B12/B13/ B18/B19/B20/B25/B26/ B28/B66/B71/B85		GLONASS, BeiDou/Compass, Galileo, QZSS
BG95-M4*	**Cat M1:** LTE-FDD: B1/B2/B3/B4/B5/B8/B12/B13/ B14/B18/B19/B20/B25/B26/B27/ B28/B31/B66/B72/B73/B85 **Cat NB2:** LTE-FDD: B1/B2/B3/B4/B5/B8/B12/B13/ B18/B19/B20/B25/B26/B28/B31/ B66/B72/B73/B85	Power Class 5 (21dBm)	GPS, GLONASS, BeiDou/Compass, Galileo, QZSS
BG95-M5*	**Cat M1:** LTE-FDD: B1/B2/B3/B4/B5/B8/B12/B13/ B14/B18/B19/B20/B25/B26/B27/ B28/B66/B85 **Cat NB2:** LTE-FDD: B1/B2/B3/B4/B5/B8/B12/B13/ B18/B19/B20/B25/B26/B28/B66/ B71/B85 **EGPRS:** 850/900/1800/1900MHz	Power Class 3 (23dBm)	GPS, GLONASS, BeiDou/Compass, Galileo, QZSS
BG95-MF [4)]	**Cat M1:** LTE-FDD: B1/B2/B3/B4/B5/B8/B12/B13/ B14/B18/B19/B20/B25/B26/B27/ B28/B66/B85 **Cat NB2:** LTE-FDD: B1/B2/B3/B4/B5/B8/B12/B13/ B18/B19/B20/B25/B26/ B28/B66/B71/B85 **Wi-Fi (For Positioning Only):** 2.4GHz	Power Class 5 (21dBm)	GPS, GLONASS, BeiDou/Compass, Galileo, QZSS

NOTES

1. [1)] GNSS function of BG96 is optional.
2. [2)] BG96 supports VoLTE (Voice over LTE) under LTE Cat M1. BG95 supports VoLTE (Voice over

LTE) under LTE Cat M1 and CS voice under GSM. The voice function of BG95 is under development.
3. [3] LTE Cat NB2 is backward compatible with LTE Cat NB1.
4. [4] BG95-MF are under planning. Details of them are currently not included and will be added in a future release of this document.
5. [5] LTE B25 is supported on BG96 with R1.2 hardware version.
6. "*" means under development.

2.2. Features Overview

The following table compares general features of BG95 and BG96 modules.

Table 3: Features Overview

Feature	BG96	BG95
Power Supply	3.3V to 4.3V Typ. 3.8V	**BG95-M1/-M2/-N1:** 2.6V [1] to 4.8V, Typ. 3.3V **BG95-M3/-M5:** 3.3V~4.3V, Typ. 3.8V **BG95-M4:** Typ. 3.8V
Peak Current	**VBAT_BB:** Max 0.8 A **VBAT_RF:** Max 1.8 A	TBD
PSM Current	Typ. 10 μA	Typ. 3.9 μA
Sleep Current	0.8 mA @ Rock Bottom [2] **LTE Cat M1:** 1.5 mA @ DRX=1.28s 1.2 mA @ e-I-DRX=40.96s **LTE Cat NB1:** 1.96 mA @ DRX=1.28s 1.1 mA @ e-I-DRX=40.96s **2G:** 2.0 mA	0.7 mA @ Rock Bottom [2] **LTE Cat M1:** 1.65 mA @ DRX=1.28s 0.85 mA @ e-I-DRX=81.92s **LTE Cat NB1:** 1.56 mA @ DRX=1.28s 0.81 mA @ e-I-DRX=81.92s **2G:** 2.0 mA
LTE-FDD	Supported	Supported
LTE-TDD	Supported (B39)	Not supported
EDGE	Multi-slot class 33	Multi-slot class 33

GPRS	Multi-slot class 33	Multi-slot class 33
Temperature Range	Operation temperature range: -35 to +75°C [3)] Extended temperature range: -40 to +85°C [4)] Storage temperature range: -40 to +90°C	Operation temperature range: -35 to +75°C [3)] Extended temperature range: -40 to +85°C [4)] Storage temperature range: -40 to +90°C
Main UART Interface	**Baud rates:** 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps, 230400 bps, 460800 bps, 921600 bps, 115200 bps by default **Flow control:** RTS/CTS **Signal level:** 1.8V	**Baud rates:** 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps, 230400 bps, 460800 bps, 921600 bps, 115200 bps by default **Flow control:** RTS/CTS **Signal level:** 1.8V
USB Interface	USB 2.0 (Slave only) Full speed and high speed	USB 2.0 (Slave only) Low speed and full speed
Digital Audio	PCM	PCM*
I2C Interface	Supported	Supported*
ADC	Two ADCs	Two ADCs [5)]
RTC Backup	Not supported	Not supported
(U)SIM Card Detection	Supported	Supported*
Firmware Upgrade	USB, DFOTA	USB, DFOTA*

NOTES

1. [1)] For every VBAT transition/re-insertion from 0V, the minimum power supply voltage should be more than 2.7V. Meanwhile, in order to guarantee stability and RF performance, the minimum power supply voltage should be more than 2.8V. After the module starts up normally, the minimum safety voltage is 2.6V.
2. [2)] means the operation is performed with **AT+CFUN=0** and **AT+QSCLK=1** (DTR pin at high level).
3. [3)] Within operation temperature range, the module is 3GPP compliant.
4. [4)] Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to normal operation temperature levels, the module will meet 3GPP specifications again.

5. [5)] BG95 supports ADC0 and ADC1. The two interfaces are internally connected, therefore they cannot be used simultaneously. If the two ADC interfaces are intended to be used at the same time, please add an external analog switch.
6. "*" means under development.

3 Pin Definition

3.1. Pin Assignment

The following figure shows the pin assignment of BG96 and BG95.

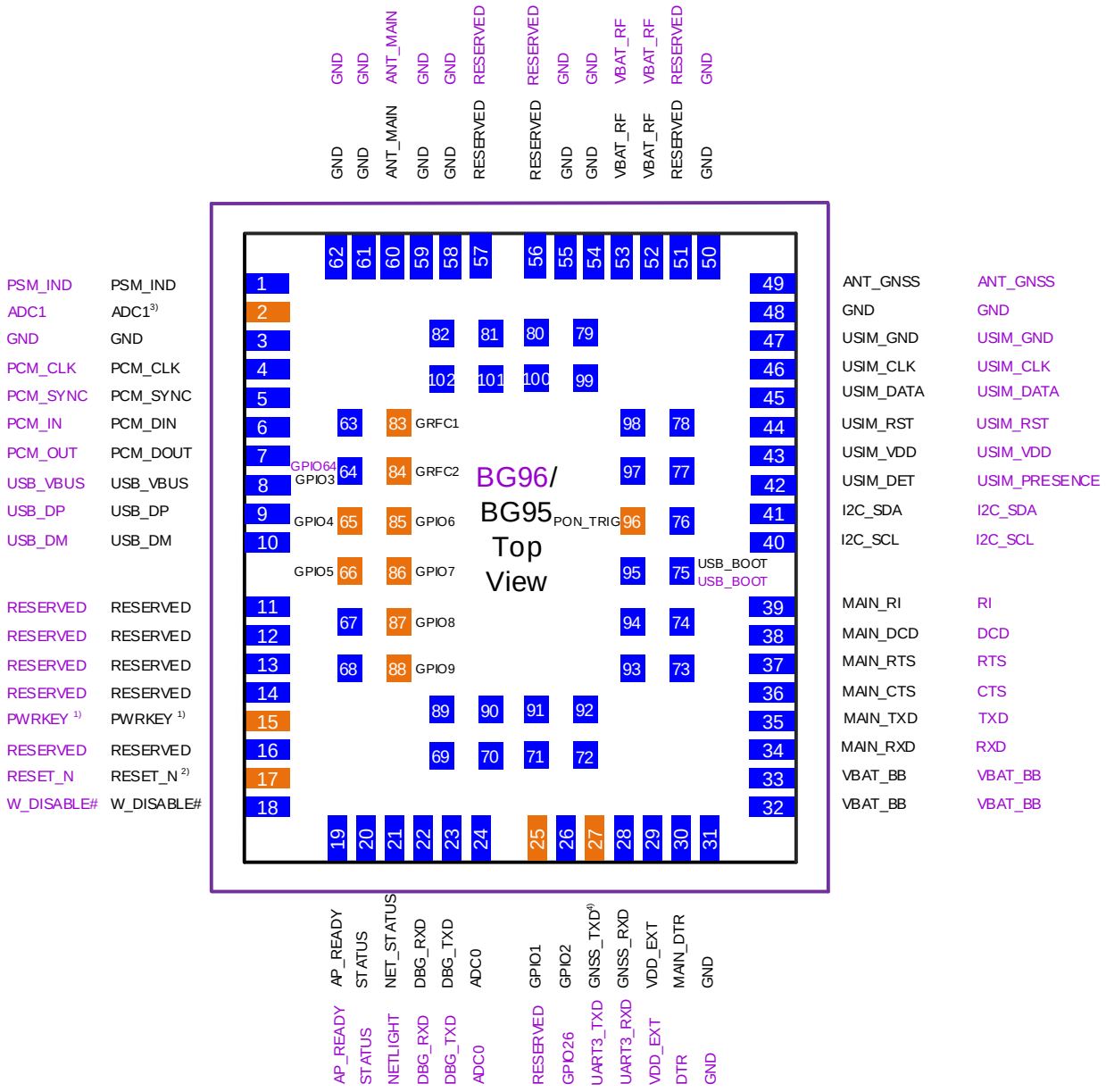


Figure 1: BG96&BG95 Pin Assignment

NOTES

1. [1] PWRKEY is internally pulled up to an internal voltage in the Qualcomm chipset, and its output voltage is the internal voltage minus a diode drop in the chipset. For BG95, the expected output voltage of PWRKEY is 1.5V, and PWRKEY should never be pulled down to GND permanently. For BG96, the expected output voltage of PWRKEY is 0.8V.
2. [2] BG95 can be reset by driving RESET_N low for 2s to 3.8s. BG96 can be reset by driving RESET_N low for 150ms to 460ms.
3. [3] BG95 supports ADC0 and ADC1. The two interfaces are internally connected, therefore they cannot be used simultaneously. If the two ADC interfaces are intended to be used at the same time, please add an external analog switch.
4. [4] GNSS_TXD of BG95 is a BOOT_CONFIG pin, and it cannot be pulled up before startup.
5. The black colored pin names are defined for BG95. The purple colored pin names are defined for BG96.
6. The orange color indicates the pins with different functions between BG95 and BG96.
7. "*" means under development.

3.2. Pin Definition

This chapter describes the pin definition of BG95 and BG96 as well as the pin comparison of them.

Table 4: I/O Parameters Definition

Type	Description
AI	Analog input
AO	Analog output
DI	Digital input
DO	Digital output
IO	Bidirectional
OD	Open drain
PI	Power input
PO	Power output

Table 5: Pin Definition Comparison between BG96 and BG95

Pin No.	BG96			BG95		
	Pin Name	I/O	Description	Pin Name	I/O	Description
1	PSM_IND [1)]	DO	Power saving mode indication. 1.8V power domain.	PSM_IND [1)]	DO	Power saving mode indication. 1.8V power domain
2	ADC1	AI	General-purpose analog to digital converter interface. Voltage range: 0.3V~1.8V.	ADC1 [2)]	AI	General-purpose analog to digital converter interface. Voltage range: 0.3V~1.8V.
3	GND	/	Ground	GND	/	Ground
4	PCM_CLK	DO	PCM clock output. 1.8V power domain.	PCM_CLK	DO	PCM clock output. 1.8V power domain.
5	PCM_SYNC	DO	PCM frame synchronization output. 1.8V power domain.	PCM_SYNC	DO	PCM frame synchronization output. 1.8V power domain.
6	PCM_IN	IO	PCM data input. 1.8V power domain.	PCM_DIN	IO	PCM data input. 1.8V power domain.
7	PCM_OUT	IO	PCM data output. 1.8V power domain.	PCM_DOUT	IO	PCM data output. 1.8V power domain.
8	USB_VBUS	AI	USB detection. 3.0V~5.25V.	USB_VBUS	AI	USB detection. Typ. 5.0V.
9	USB_DP	IO	USB differential data bus (+). 90Ω differential impedance.	USB_DP	IO	USB differential data bus (+). 90Ω differential impedance.
10	USB_DM	IO	USB differential data bus (-). 90Ω differential impedance.	USB_DM	IO	USB differential data bus (-). 90Ω differential impedance.
11~14	RESERVED	/	/	RESERVED	/	/
15	PWRKEY [3)]	DI	Turn on/off the module	PWRKEY [3)]	DI	Turn on/off the module
16	RESERVED	/	/	RESERVED	/	/

17	RESET_N	DI	Reset signal of the module. 1.8V power domain.	RESET_N [4)]	DI	Reset signal of the module. 1.8V power domain.
18	W_DISABLE#	DI	Airplane mode control. 1.8V power domain.	W_DISABLE#	DI	Airplane mode control. 1.8V power domain.
19	AP_READY	DI	Application processor sleep state detection. 1.8V power domain.	AP_READY	DI	Application processor sleep state detection. 1.8V power domain.
20	STATUS	DO	Indicate the module's operation status. 1.8V power domain.	STATUS	DO	Indicate the module's operation status. 1.8V power domain.
21	NETLIGHT	DO	Indicate the module's network activity status. 1.8V power domain.	NET_STATUS	DO	Indicate the module's network activity status. 1.8V power domain.
22	DBG_RXD	DI	Receive data. 1.8V power domain	DBG_RXD	DI	Receive data. 1.8V power domain
23	DBG_TXD	DO	Transmit data. 1.8V power domain.	DBG_TXD	DO	Transmit data. 1.8V power domain.
24	ADC0	AI	General-purpose analog to digital converter interface Voltage range: 0.3V~1.8V.	ADC0 [3)]	AI	General-purpose analog to digital converter interface Voltage range: 0.3V~1.8V.
25	RESERVED	/	/	GPIO1	IO	General-purpose input and output 1.8V power domain
26	GPIO26	IO	General-purpose input and output. 1.8V power domain.	GPIO2	IO	General-purpose input and output. 1.8V power domain.
27	UART3_TXD	DO	Transmit data. 1.8V power domain.	GNSS_TXD	DO	Transmit data. 1.8V power domain.

28	UART3_RXD	DI	Receive data. 1.8V power domain.	GNSS_RXD	DI	Receive data. 1.8V power domain.
29	VDD_EXT	PO	Provide 1.8V for external circuit	VDD_EXT	PO	Provide 1.8V for external circuit
30	DTR	DI	Data terminal ready. Sleep mode control. 1.8V power domain.	MAIN_DTR	DI	Data terminal ready. Sleep mode control. 1.8V power domain.
31	GND	/	Ground	GND	/	Ground
32~33	VBAT_BB	PI	Power supply for the module's baseband part: 3.3V~4.3V, typ. 3.8V	VBAT_BB	PI	Power supply for module's baseband part: **BG95-M1/-M2/-N1:** 2.6V [5]~4.8V, Typ. 3.3V **BG95-M3/-M5:** 3.3V~4.3V, Typ. 3.8V **BG95-M4:** Typ. 3.8V
34	RXD	DI	Receive data. 1.8V power domain.	MAIN_RXD	DI	Receive data. 1.8V power domain.
35	TXD	DO	Transmit data. 1.8V power domain.	MAIN_TXD	DO	Transmit data. 1.8V power domain.
36	CTS	DO	Clear to send. 1.8V power domain.	MAIN_CTS	DO	Clear to send. 1.8V power domain.
37	RTS	DI	Request to send. 1.8V power domain.	MAIN_RTS	DI	Request to send. 1.8V power domain.
38	DCD	DO	Data carrier detection. 1.8V power domain.	MAIN_DCD	DO	Data carrier detection. 1.8V power domain.
39	RI	DO	Ring indication. 1.8V power domain.	MAIN_RI	DO	Ring indication. 1.8V power domain.
40	I2C_SCL	OD	I2C serial clock. Used	I2C_SCL	OD	I2C serial clock.

			for external codec. Require external pull-up to 1.8V.			Used for external codec. Require external pull-up to 1.8V.
41	I2C_SDA	OD	I2C serial data. Used for external codec. Require external pull-up to 1.8V.	I2C_SDA	OD	I2C serial data. Used for external codec. Require external pull-up to 1.8V.
42	USIM_ PRESENCE	DI	(U)SIM card hot-plug detect. 1.8V power domain.	USIM_DET	DI	(U)SIM card hot-plug detect. 1.8V power domain.
43	USIM_VDD	PO	Power supply for (U)SIM card. 1.8V/3.0V	USIM_VDD	PO	Power supply for (U)SIM card. 1.8V
44	USIM_RST	DO	Reset signal of (U)SIM card. 1.8V/3.0V(U)SIM card supported.	USIM_RST	DO	Reset signal of (U)SIM card. Only 1.8V (U)SIM card supported.
45	USIM_DATA	IO	Data signal of (U)SIM card. 1.8V/3.0V(U)SIM card supported.	USIM_DATA	IO	Data signal of (U)SIM card. Only 1.8V (U)SIM card supported.
46	USIM_CLK	DO	Clock signal of (U)SIM card. 1.8V/3.0V(U)SIM card supported.	USIM_CLK	DO	Clock signal of (U)SIM card. Only 1.8V (U)SIM card supported.
47	USIM_GND	/	Specified ground for (U)SIM card	USIM_GND	/	Specified ground for (U)SIM card
48	GND	/	Ground	GND	/	Ground
49	ANT_GNSS	AI	GNSS antenna interface	ANT_GNSS	AI	GNSS antenna interface
50	GND	/	Ground	GND	/	Ground
51	RESERVED	/	/	RESERVED	/	/
52~53	VBAT_RF	PI	Power supply for the module's RF part: 3.3V~4.3V, typ. 3.8V	VBAT_RF	PI	Power supply for the module's RF part: **BG95-M1/-M2/-N1:** 2.6V [5]~4.8V, Typ. 3.3V **BG95-M3/-M5:**

						3.3V~4.3V, Typ. 3.8V **BG95-M4:** Typ. 3.8V
54	GND	/	Ground	GND	/	Ground
55	GND	/	Ground	GND	/	Ground
56	RESERVED	/	/	RESERVED	/	/
57	RESERVED	/	/	RESERVED	/	/
58	GND	/	Ground	GND	/	Ground
59	GND	/	Ground	GND	/	Ground
60	ANT_MAIN	IO	Main antenna interface	ANT_MAIN	IO	Main antenna interface
61	GND	/	Ground	GND	/	Ground
62	GND	/	Ground	GND	/	Ground
63	RESERVED	/	/	RESERVED	/	/
64	GPIO64	IO	General-purpose input/output interface. 1.8V power domain.	GPIO3	IO	General-purpose input/output interface. 1.8V power domain.
65	RESERVED	/	/	GPIO4	IO	General-purpose input/output interface
66	RESERVED	/	/	GPIO5	IO	General-purpose input/output interface
75	USB_BOOT	DI	Force the module to boot from USB port. 1.8V power domain.	USB_BOOT	DI	Force the module to boot from USB port. 1.8V power domain.
83	RESERVED	/	/	GRFC1	DO	Generic RF Controller interface. 1.8V power domain.
84	RESERVED	/	/	GRFC2	DO	Generic RF Controller

						interface. 1.8V power domain.
85	RESERVED	/	/	GPIO6	IO	General-purpose input/output interface. 1.8V power domain.
86	RESERVED	/	/	GPIO7	IO	General-purpose input/output interface. 1.8V power domain.
87	RESERVED	/	/	GPIO8	IO	General-purpose input/output interface. 1.8V power domain.
88	RESERVED	/	/	GPIO9	IO	General-purpose input/output interface. 1.8V power domain.
76~78, 92~95, 97~99	RESERVED	/	/	RESERVED	/	/
96	RESERVED	/	/	PON_TRIG	DI	Wake up the module from PSM
67~74, 79~82, 89~91, 100~102	GND	/	Ground	GND	/	Ground

NOTES

1. [1)] When PSM is enabled, the function of PSM_IND pin will be activated after the module is rebooted. When PSM_IND is in high voltage level, the module is in normal operation state, and when it is in low voltage level, the module is in PSM.
2. [2)] BG95 supports ADC0 and ADC1. The two interfaces are internally connected, therefore they cannot be used simultaneously. If the two ADC interfaces are intended to be used at the same time, please add an external analog switch.
3. [3)] PWRKEY is internally pulled up to an internal voltage in the Qualcomm chipset, and its output

voltage is the internal voltage minus a diode drop in the chipset. For BG95, the expected output voltage of PWRKEY is 1.5V, and PWRKEY should never be pulled down to GND permanently. For BG96, the expected output voltage of PWRKEY is 0.8V.

4. [4)] BG95 can be reset by driving RESET_N low for 2s to 3.8s. BG96 can be reset by driving RESET_N low for 150ms to 460ms.
5. [5)] For every VBAT transition/re-insertion from 0V, the minimum power supply voltage should be more than 2.7V. Meanwhile, in order to guaranteed stability and RF performance, the minimum power supply voltage should be more than 2.8V. After the module startup normally, the minimum safety voltage is 2.6V.
6. PSM_IND, W_DISABEL#, AP_READY, USIM_DET, PCM, I2C, GRFC and GPIO functions of BG95 are under development.
7. Keep all reserved and unused pins unconnected.
8. All GND pins should be connected to ground.
9. "*" means under development.

4 Hardware Reference Designs

The following chapters describe the compatible design between BG95 and BG96 on main functionalities.

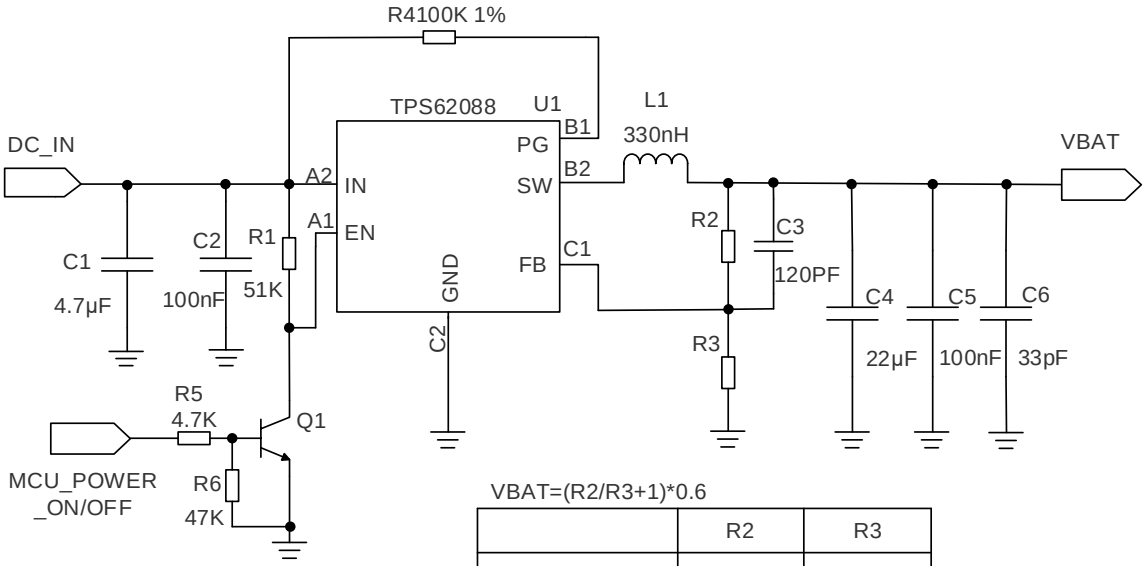
4.1. Power Supply

4.1.1. Reference Design for Power Supply

Power design for a module is critical to its performance. BG95 and BG96 are LPWA modules requiring low quiescent and leakage current, and also support 2G network. So the power IC must be able to provide sufficient current output for 2G network.

If the voltage drop between the input and output is not too high, it is recommended to use an LDO to supply power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is preferred to be used as the power supply.

The following is a power supply reference design of BG95/BG96 where buck converter solution is used.



VBAT=(R2/R3+1)*0.6

	R2	R3
BG95-M3/-M4/-M5	536kΩ 1%	100kΩ 1%
BG95-M1/-M2/-N1	453kΩ 1%	100kΩ 1%

Figure 2: Reference Circuit of Power Supply (BG95/BG96)

Special attention should be paid to the power supply design for BG95/BG96:

- If only LTE Cat M1 and Cat NB1 networks are intended to be used, it is recommended to select a DC-DC chip or LDO chip with ultra-low leakage current and current output no less than 1.0A as the power supply.

- If LTE Cat M1, Cat NB1 and EGPRS networks are all intended to be used, the current output of DC-DC chip or LDO chip cannot be lower than 2.0A and power supply chips with low leakage current should be selected because the module needs more current when transmitting in 2G condition.

4.1.2. Reduce Voltage Drop

The power supply range of BG95 and BG96 modules are listed below:

- **BG96 and BG95-M3/-M5:** 3.3V to 4.3V, typ. 3.8V
- **BG95-M1/-M2/-N1:** 2.6V to 4.8V, typ. 3.3V
- **BG95-M4:** typ. 3.8V

Please make sure the input voltage never drop below 3.3V or exceed 4.2V in BG95 and BG96 compatible design. The VBAT to BG95/BG96 module's VBAT_BB and VBAT_RF pins should be divided into two separated paths in star structure.

In addition, in order to avoid the damage caused by electric surge and ESD, it is suggested that a TVS diode with low reverse stand-off voltage (V_{RWM}), low leakage current, low clamping voltage (V_C) and high reverse peak pulse current (I_{PP}) should be used.

The following figure shows a reference design of VBAT for BG95 and BG96.

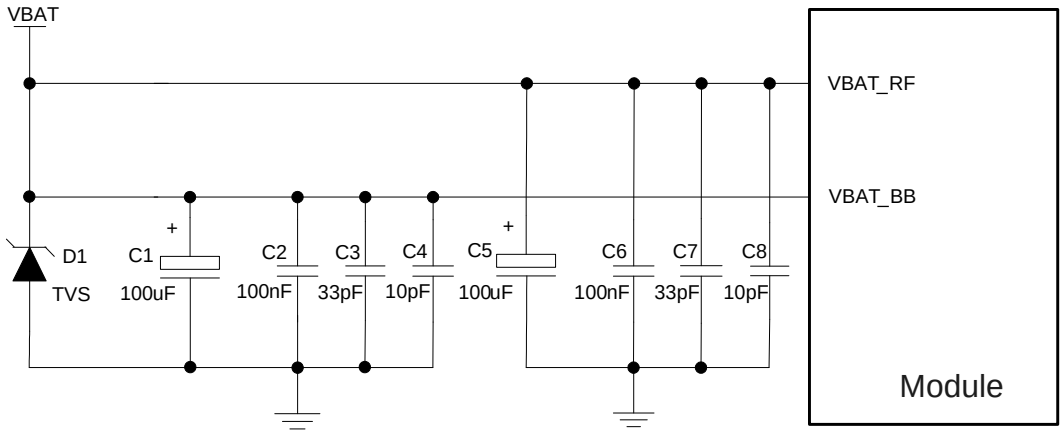


Figure 3: Reference Circuit of VBAT (BG95/BG96)

4.2. Turn-on

The turn-on method of BG95 is the same as that of BG96. BG95 can be powered on through pressing PWRKEY for **500ms to 1000ms**, and BG96 can be powered on through pressing PWRKEY for **at least 500ms**.

The PWRKEY pin of BG95/BG96 is internally pulled up to an internal voltage in the Qualcomm chipset, and its output voltage is the internal voltage minus a diode drop in the chipset. For BG95, the expected output voltage of PWRKEY is **1.5V**. For BG96, the expected output voltage of PWRKEY is **0.8V**.

The following is a reference design for the turn-on circuit of BG95 and BG96.

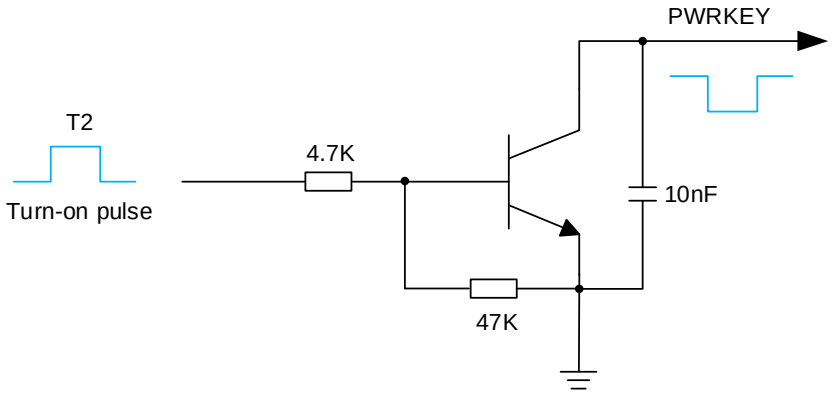


Figure 4: PWRKEY Driving Circuit for Module Turn-on (BG95/BG96)

The power-on scenario of BG95 and BG96 is illustrated in the figure below.

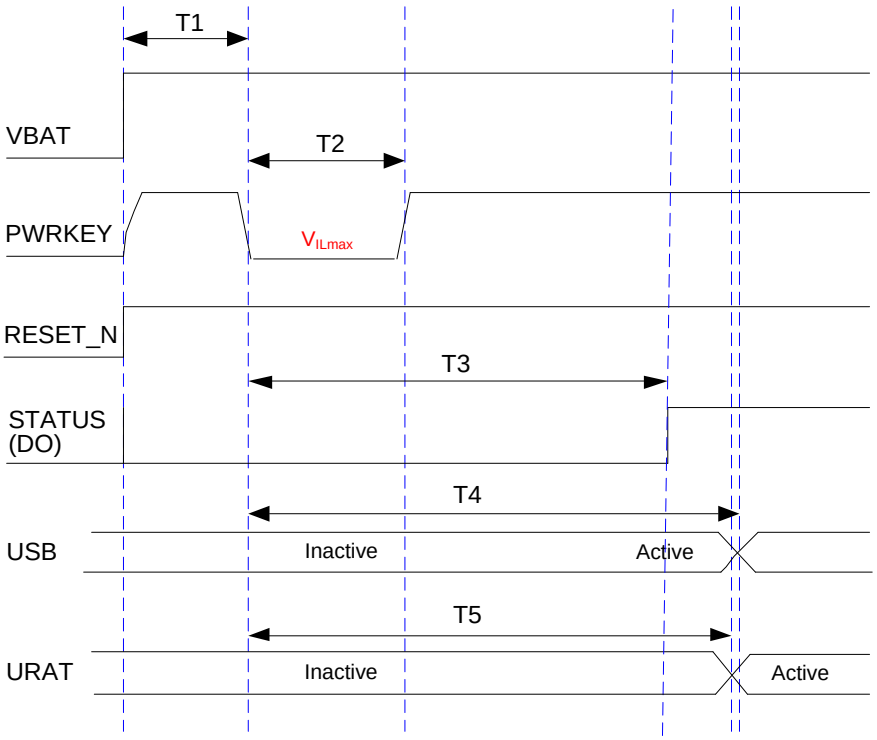


Figure 5: Power-on Scenario (BG95/BG96)

Table 6: Power-on Timing of BG95/BG96

Module	T_1	T_2	T_3	T_4	T5	V_{ILmax}
BG96	≥30ms	≥500ms	≥4.8s	≥4.2s	≥4.9s	≤0.5V
BG95	≥30ms	500ms~1s	2.1s Typ.	2.55s Typ.	2.5s Typ.	≤0.45V

NOTES

1. For BG95, PWRKEY should never be pulled down to GND permanently.
2. Please make sure that VBAT is stable before pulling down PWRKEY pin, and T_1 is recommended to be more than 30ms.

4.3. Turn-off

4.3.1. Turn off Module via AT Command (BG95/BG96)

There are several ways to turn off BG95/BG96. It is recommended to turn off the module through **AT+QPOWD** command, which a safe way. The command will make the module log out from the network and allow the firmware to save important data before completely disconnecting the power supply.

The power-off scenario of BG95/BG96 is illustrated in the figure below.

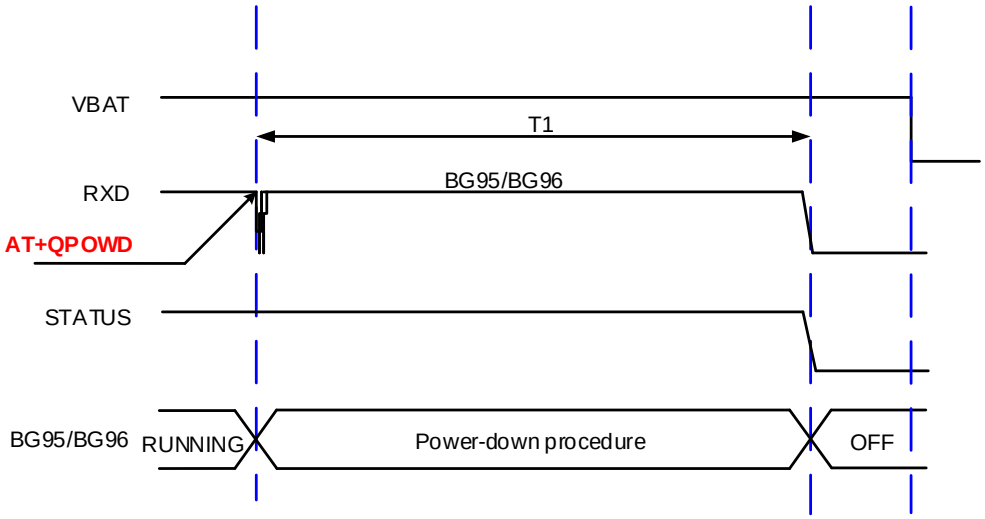


Figure 6: Power-off Scenario through AT Command (BG95/BG96)

Table 7: Power-off Timing by AT Command of BG95/BG96

Module	T_1
BG96	≥2s
BG95	≥1.3s

4.3.2. Turn off Module by PWRKEY and VBAT (BG95/BG96)

It is also a safe way to turn off the modules by driving PWRKEY low for **650ms to 1500ms** for BG95, and **at least 650ms** for BG96.

The power-off scenario of BG95 and BG96 by PWRKEY is illustrated in the figure below.

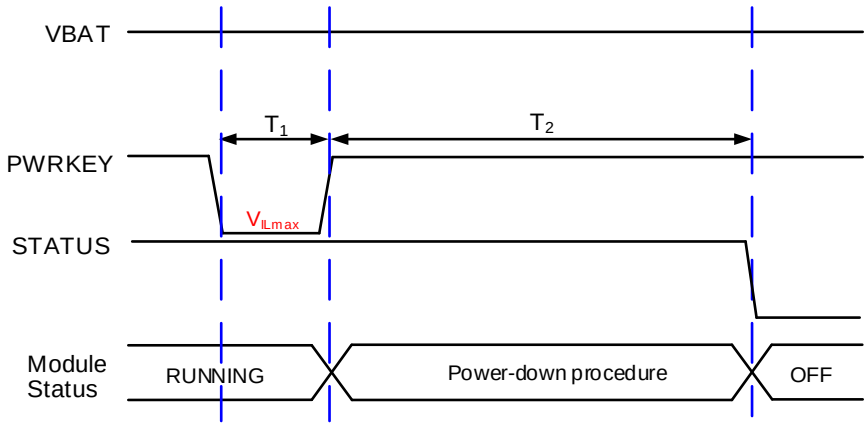


Figure 7: Power-off Scenarios by PWRKEY (BG95/BG96)

Table 8: Power-off Timing by PWRKEY (BG95/BG96)

Module	V_{ILmax}	T_1	T_2
BG96	≤0.5V	≥650ms	≥2s
BG95	≤0.45V	650ms~1.5s	≥1.3s

4.4. Reset

BG95 can be reset by driving RESET_N low for **2s to 3.8s**. BG96 can be reset by driving RESET_N low for **150ms to 460ms**.

The recommended circuits for RESET_N control are shown below and they are similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET_N pin.

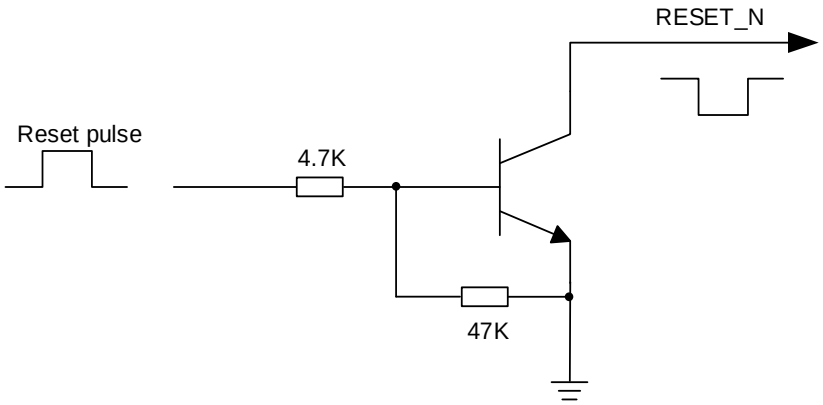


Figure 8: Reference Circuit of RESET_N by Using Driving Circuit (BG95/BG96)

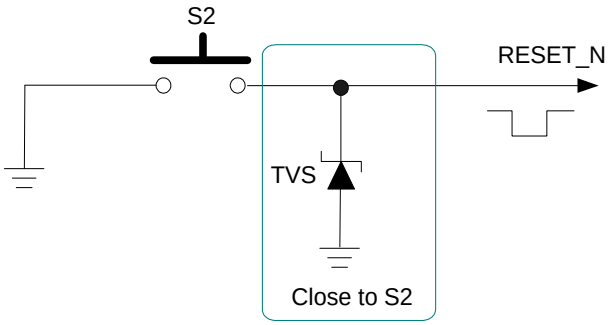


Figure 9: Reference Circuit of RESET_N by Using Button (BG95/BG96)

The reset scenario of BG95 and BG96 is illustrated in the figure below.

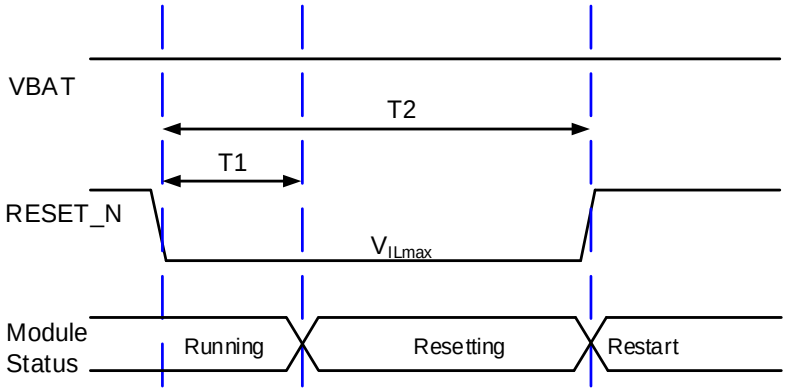


Figure 10: Reset Scenario (BG95/BG96)

Table 7: Reset Timing of BG95/BG96

Module	V_{ILmax}	T_1	T_2
BG96	≤0.5V	≥150ms	≤460ms
BG95	≤0.45V	≥2s	≤3.8s

NOTES

1. Use RESET_N only when turning off the module by **AT+QPOWD** command and PWRKEY pin both failed.
2. Please make sure that there is no large capacitor on PWRKEY and RESET_N pins.

4.5. Network Status Indication

BG95/BG96 provides one network status indication pin: NET_STATUS/NETLIGHT. The pin is used to drive a network status indication LED. A reference circuit is shown in the following figure.

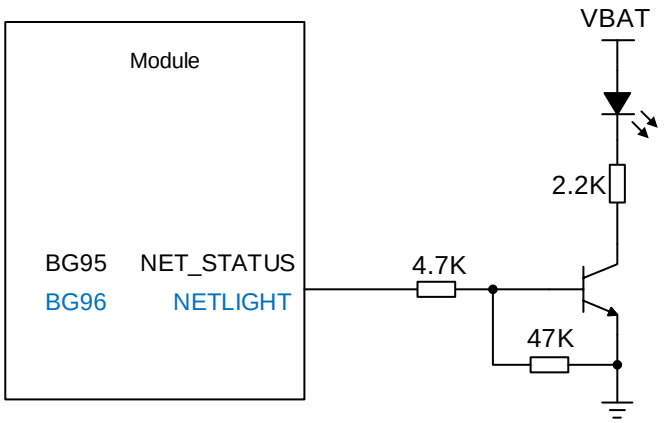


Figure 11: Reference Circuit of NETLIGHT

4.6. Operation Status Indication

BG95/BG96 provides a STATUS pin to indicate the module's operation status. STATUS will output high level when the module is powered on. The following figure shows a reference circuit of STATUS.

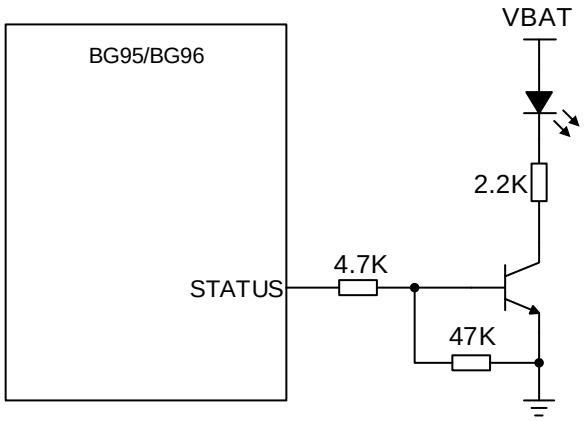


Figure 12: Reference Circuit of STATUS

4.7. (U)SIM Interface

BG95 and BG96 support one (U)SIM interface that can meets ETSI and IMT-2000 requirements. BG96 supports 1.8V/3.0V (U)SIM card, but BG95 only supports 1.8V (U)SIM card.

The following figure shows a reference design for (U)SIM interface with a 6-pin (U)SIM card connector.

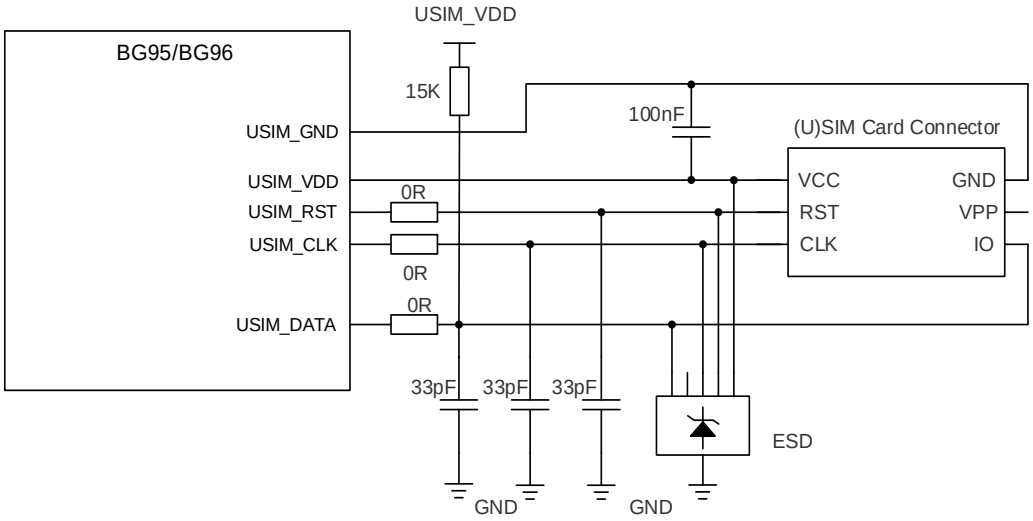


Figure 13: Reference Circuit of (U)SIM Interface with a 6-Pin (U)SIM Card Connector

If (U)SIM card detection function needs to be used, please keep USIM_DET/USIM_PRESENCE connected. The following figure shows a reference design for (U)SIM interface with (U)SIM card detection function.

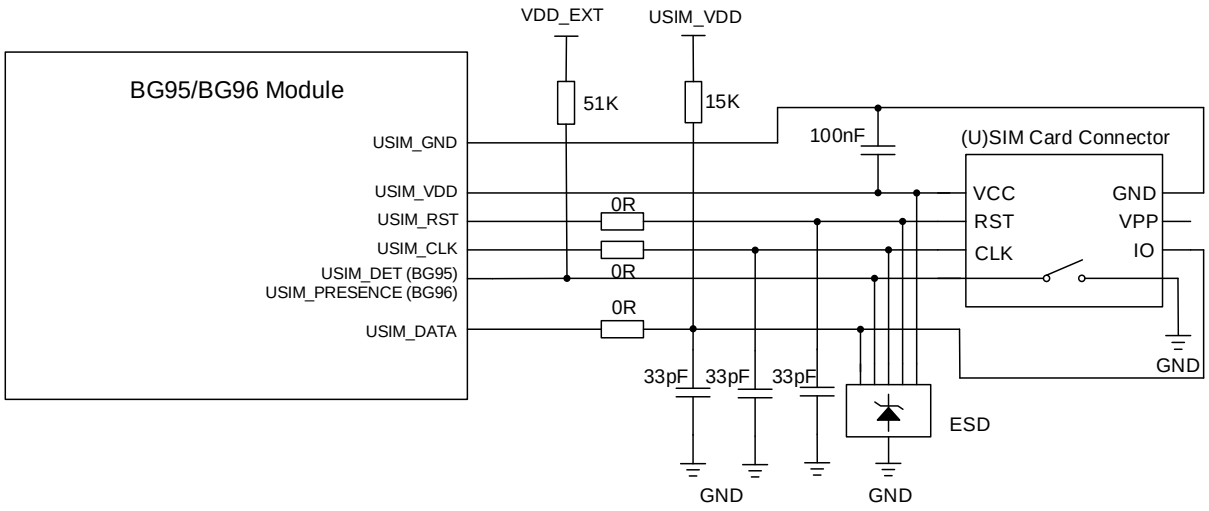


Figure 14: Reference Design of (U)SIM Card Interface with (U)SIM Card Detection

In order to enhance the reliability and availability of the (U)SIM card in applications, please follow the criteria below in (U)SIM circuit design:

- Keep the placement of (U)SIM card connector as close to the module as possible. Keep the trace length as less than 200 mm as possible.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Assure the ground between the module and the (U)SIM card connector short and wide. Keep the trace width of ground and USIM_VDD no less than 0.5 mm to maintain the same electric potential. Make sure the bypass capacitor between USIM_VDD and USIM_GND less than 1 μF, and place it as close to (U)SIM card connector as possible. If the system ground plane is complete, USIM_GND can be connected to the system ground directly.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground. USIM_RST should also be ground surrounded.
- In order to offer good ESD protection, it is recommended to add a TVS diode array with parasitic capacitance not exceeding 15 pF. In order to facilitate debugging, it is recommended to reserve series resistors for the (U)SIM signals of the module. The 33 pF capacitors are used for filtering interference of EGSM900. Please note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA line can improve anti-jamming capability when long layout trace and sensitive occasion are applied, and should be placed close to the (U)SIM card connector.

NOTES

1. eSIM function of BG95 is optional. If eSIM is selected, then the external (U)SIM cannot be used simultaneously.
2. USIM_DET function of BG95 is under development.

4.8. UART Interfaces

BG95/BG96 provides three UART interfaces: Main UART, Debug UART and GNSS UART. The main UART supports hardware flow control and is used for data transmission and AT command communication. The debug UART is used for module debugging and log output. The GNSS UART is used for GNSS data and NMEA sentence output. The default baud rate of UARTs is 115200bps.

Since the UART interface power domains of both BG95 and BG96 are 1.8V, a level translator should be used if customers' application is equipped with a 3.3V UART interface. The voltage-level translator TXS0108EPWR provided by *Texas Instruments* is recommended. Please visit http://www.ti.com for more information.

The following figure shows a reference design. For details, please refer to ***document [1]*** and ***[2]***.

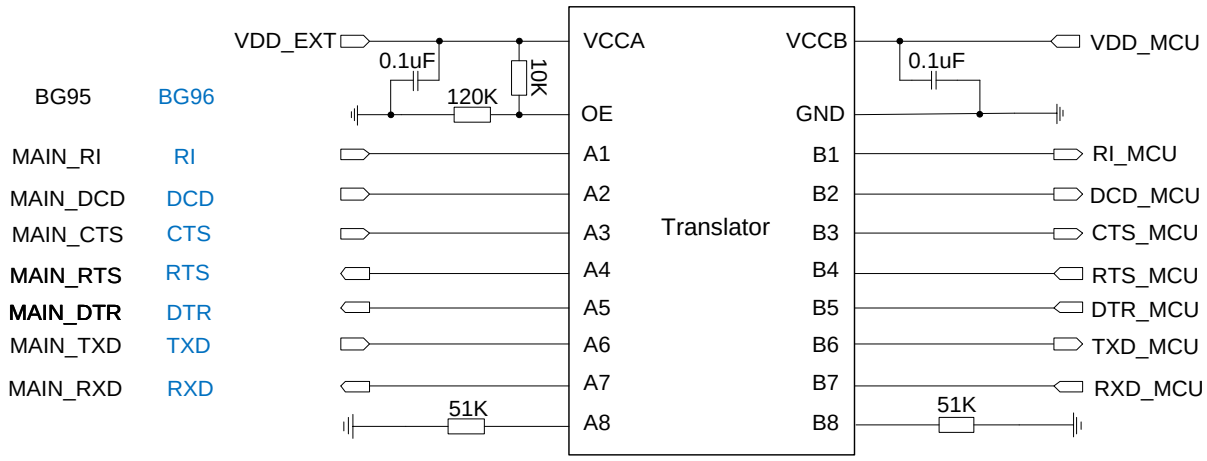


Figure 15: Reference Circuit with Translator Chip

Another example with transistor translation circuit is shown as below. For the design of circuits in dotted lines, please refer to that of circuits in solid lines, but please pay attention to the direction of connection.

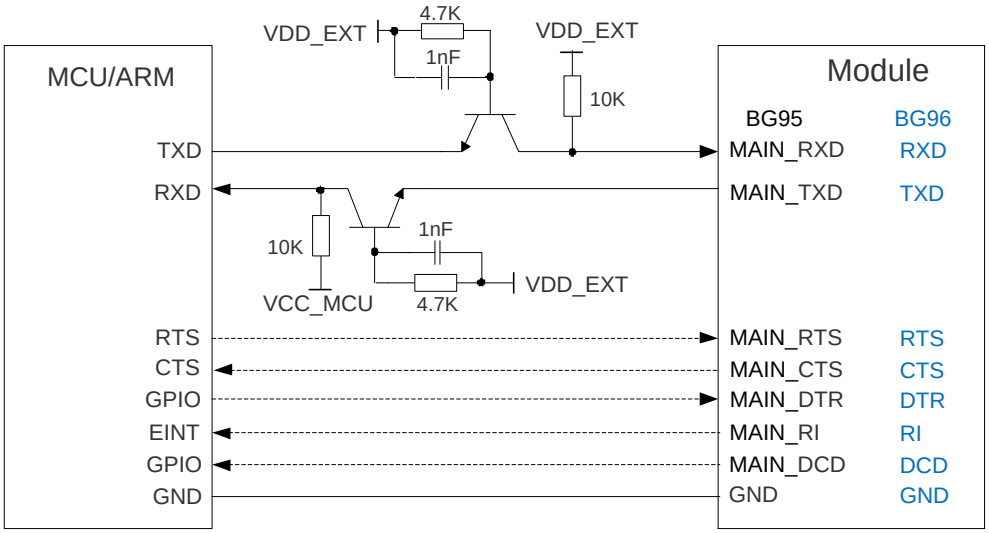


Figure 16: Reference Circuit with Transistor Circuit

NOTE

Transistor circuit solution is not suitable for applications with high baud rates exceeding 460Kbps.

4.9. USB Interface

BG95/BG96 provides one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification and supports slave mode only. BG96 supports high speed (480Mbps) and full speed (12Mbps) modes, while BG95 supports full speed (12Mbps) and low speed (1.5Mbps) modes.

The following figure shows a reference design of USB interface when application processor communicates with BG96 via USB interface.

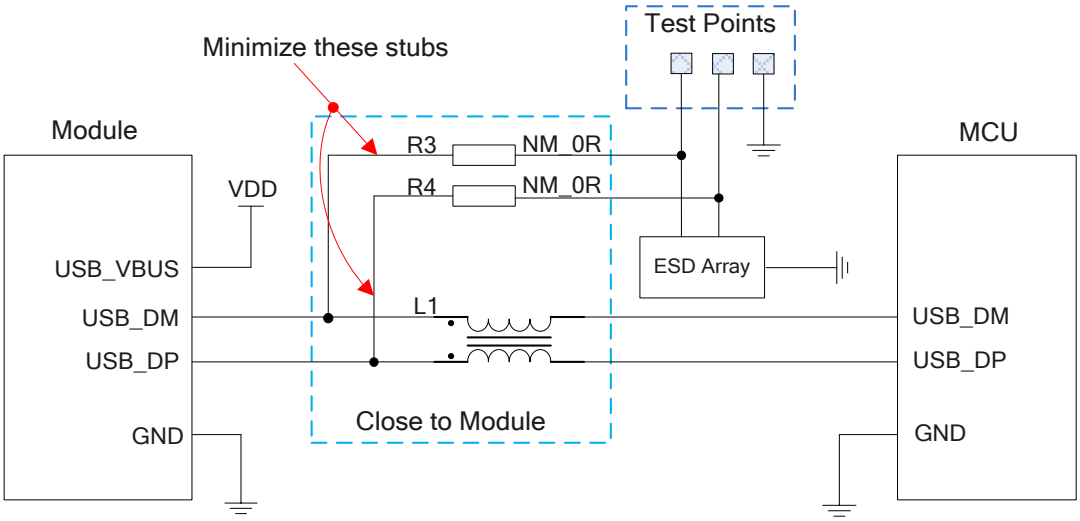


Figure 17: Reference Design of USB Interface (BG96)

The following figure shows a reference design of USB interface for BG95.

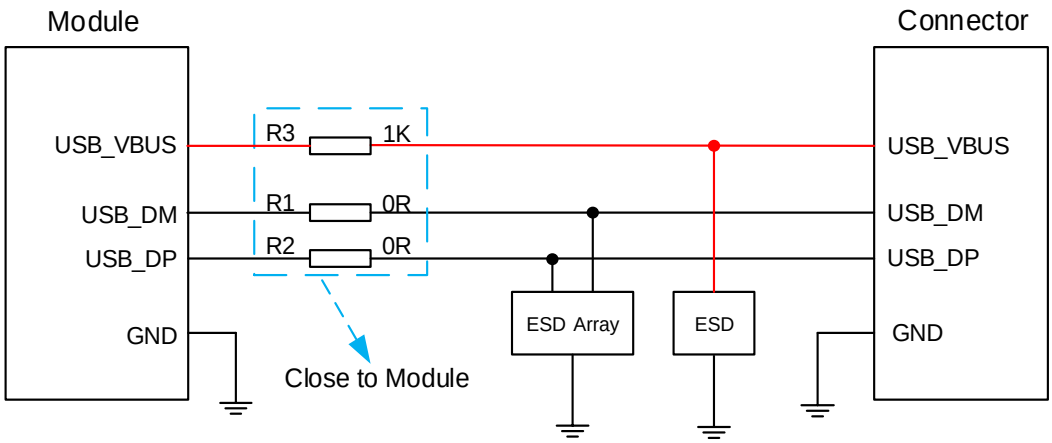


Figure 18: Reference Design of USB Interface (BG95)

For more details about the USB interfaces of BG95/BG96, please refer to ***document [1]*** and ***[2]***.

NOTES

1. BG95/BG96 can only be used as a slave device.
2. BG95 USB interface is used for AT command communication, data transmission, software debugging and firmware upgrade. However, in practical applications, the constant use of USB will result in increased power consumption. Therefore, in power-sensitive applications, it is recommended that USB is used for firmware upgrade only.

4.10. PCM and I2C Interfaces

BG95/BG96 provides one PCM digital interface and one I2C interface. A reference design of PCM and I2C interfaces with an external codec IC is shown below.

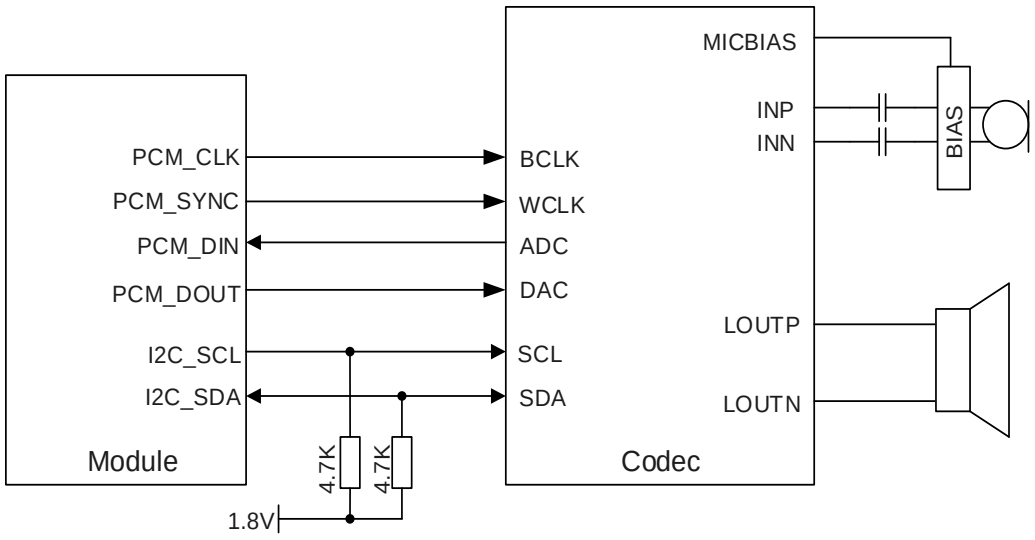


Figure 19: Reference Design of PCM Application with Audio Codec (BG95/BG96)

For more details about the PCM and I2C interfaces of BG95/BG96, please refer to ***document [1]*** and ***[2]***.

NOTE

PCM and I2C interface functions of BG95 are under development.

4.11. ADC Interfaces

BG95/BG96 provides two analog-to-digital converter (ADC) interfaces. But the ADC0 and ADC1 for BG95 are internally connected, therefore they cannot be used simultaneously. If the two ADC interfaces of BG95 are intended to be used at the same time, please add an external analog switch.

For BG95, **AT+QADC=0** command can be used to read the voltage value on the ADC being used. For more details about the AT command, please refer to ***document [3]***.

For BG96, **AT+QADC=0** command can be used to read the voltage value on ADC0 pin. **AT+QADC=1** command can be used to read the voltage value on ADC1 pin. For more details about the AT command, please refer to ***document [4]***.

For more details about the ADC interfaces of BG95/BG96, please refer to ***document [1]*** and ***[2]***.

NOTES

1. ADC input voltage must not exceed 1.8V.
2. It is prohibited to supply any voltage to ADC pins when VBAT is removed.
3. It is recommended to use resistor divider circuit for ADC application, and the divider resistor accuracy should be no less than 1%.

4.12. GPIO Interfaces*

Both BG95 and BG96 provide general-purpose input and output (GPIO) interfaces.

For BG95, the module provides nine general-purpose input and output (GPIO) interfaces. **AT+QCFG="gpio"*** command can be used to configure the status of corresponding GPIO pins. For more details about the AT command, please refer to ***document [3]***.

For BG96, the module provides two general-purpose input and output (GPIO) interfaces. **AT+QFWD** command can be used to configure corresponding GPIO pin's status. For more details about the AT command, please refer to ***document [4]***.

For more details about the GPIO interfaces of BG95/BG96, please refer to ***document [1]*** and ***[2]***.

NOTE

"*" means under development.

4.13. GRFC Interfaces*

As compared with BG96, BG95 additionally provides two general RF control interfaces for the control of external antenna tuners.

For more details about the GRFC interfaces of BG95, please refer to ***document [2]***.

NOTE

"*" means under development.

4.14. RF Antenna Interfaces

BG95/BG96 contains two RF antenna interfaces: ANT_MAIN and ANT_GNSS. The RF antenna ports has an impedance of 50Ω. In order to achieve better RF performance, a π-type matching circuit is recommended to be reserved, and π-type matching components (R1/C1/C2) should be placed as close the antenna as possible. By default, the resistance of R1 is 0Ω, and capacitors C1 & C2 are not mounted. A reference circuit for the interface is shown below.

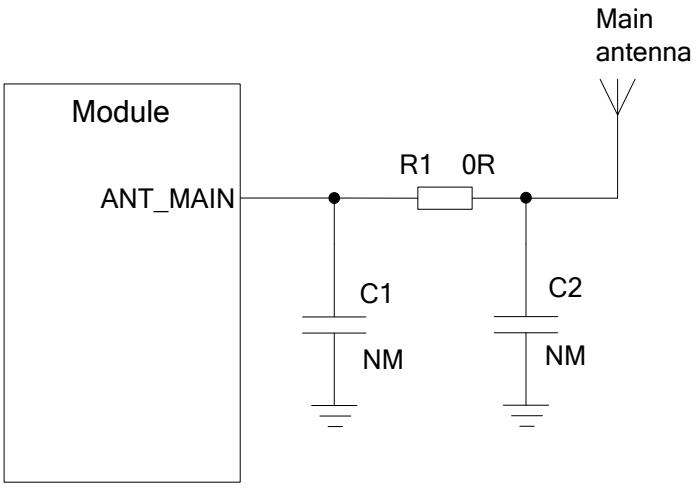


Figure 20: Reference Circuit of RF Interfaces

BG95/BG96 supports GNSS function through ANT_GNSS interface. A reference design for ANT_GNSS antenna interface of BG95/BG96 is shown as below.

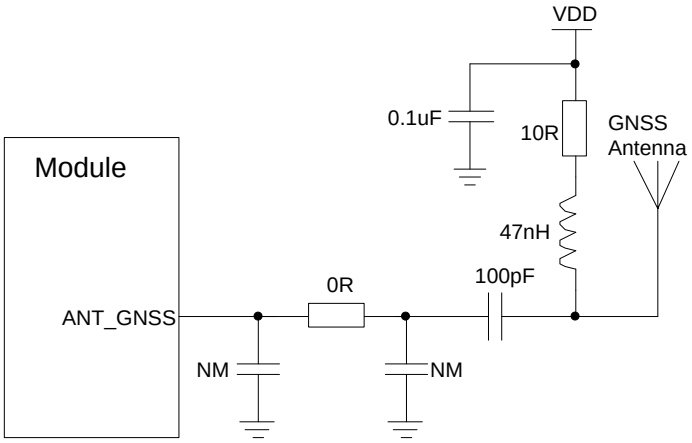


Figure 21: Reference Circuit of ANT_GNSS Interface (BG95/BG96)

NOTES

1. An external LDO can be selected to supply power according to the active antenna requirement.
2. If a passive antenna is selected, then the VDD circuit is not needed.

5 Recommended Footprint and Stencil Design

This chapter mainly introduces the recommended footprint and stencil design for BG95 and BG96 modules. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.05mm unless otherwise specified.

5.1. Recommended Compatible Footprint

The following figure shows the bottom views of BG95 and BG96.

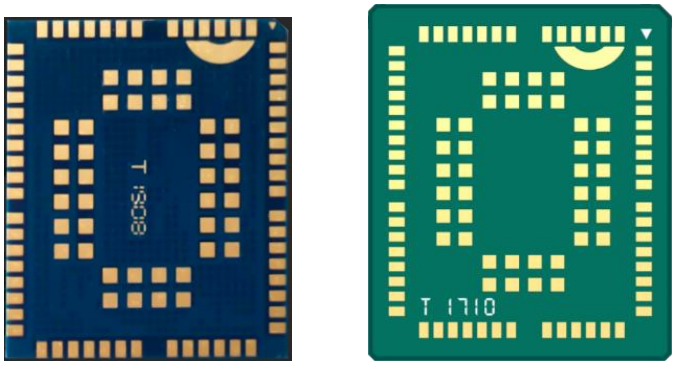


Figure 22: Bottom Views of BG95/BG96

The following figure shows the recommended compatible footprint of BG95 and BG96.

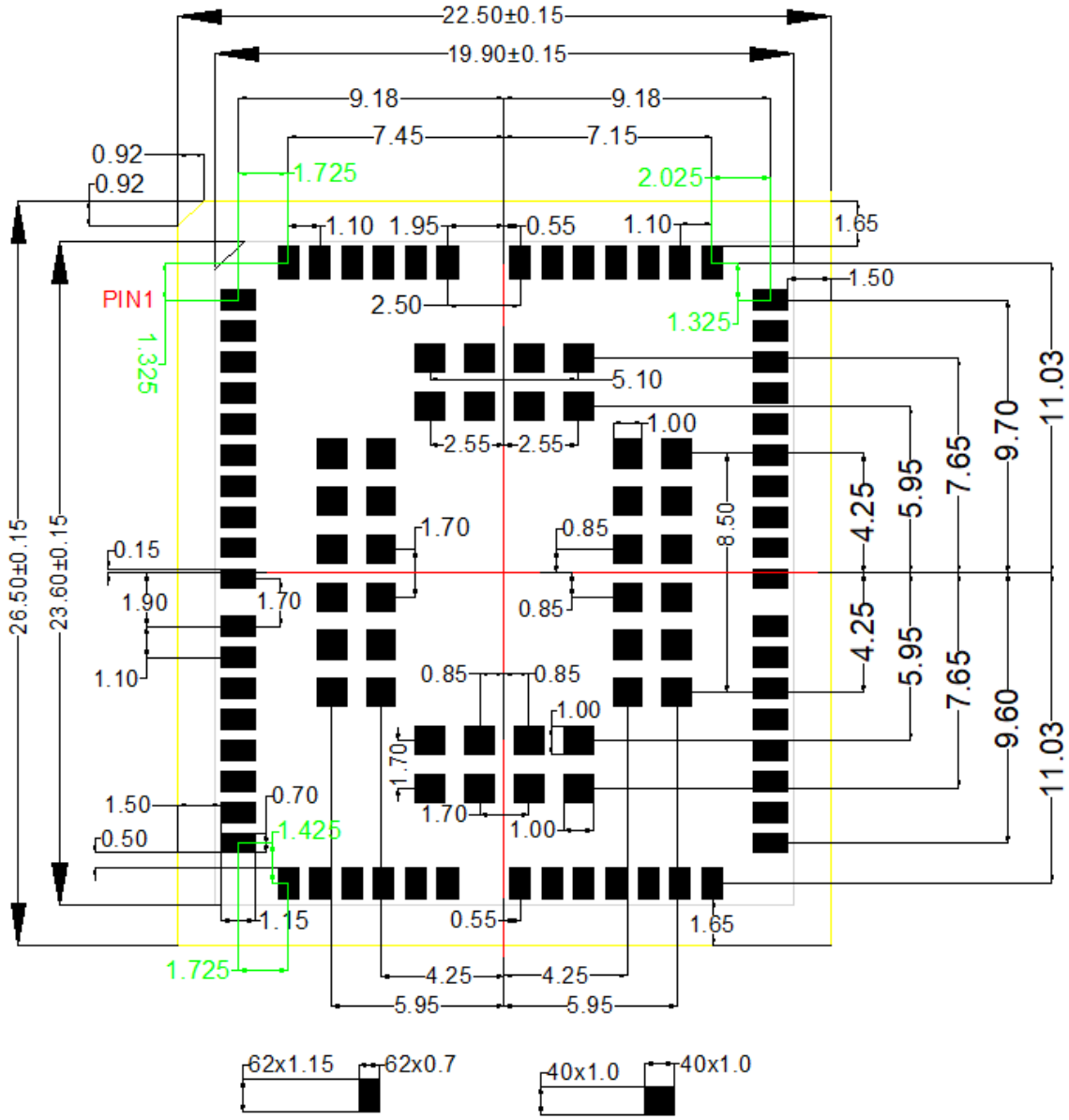


Figure 23: Recommended Footprint of BG95/BG96 (Top View)

5.2. Recommended Stencil Design

In order to ensure the module soldering quality, the thickness of stencil is recommended to be 0.13mm to 0.15mm for BG95 and BG96. For more details, please refer to ***document [5]***.

5.3. Installation Sketch Map

The following figure shows the sketch map of installation for BG95 and BG96.

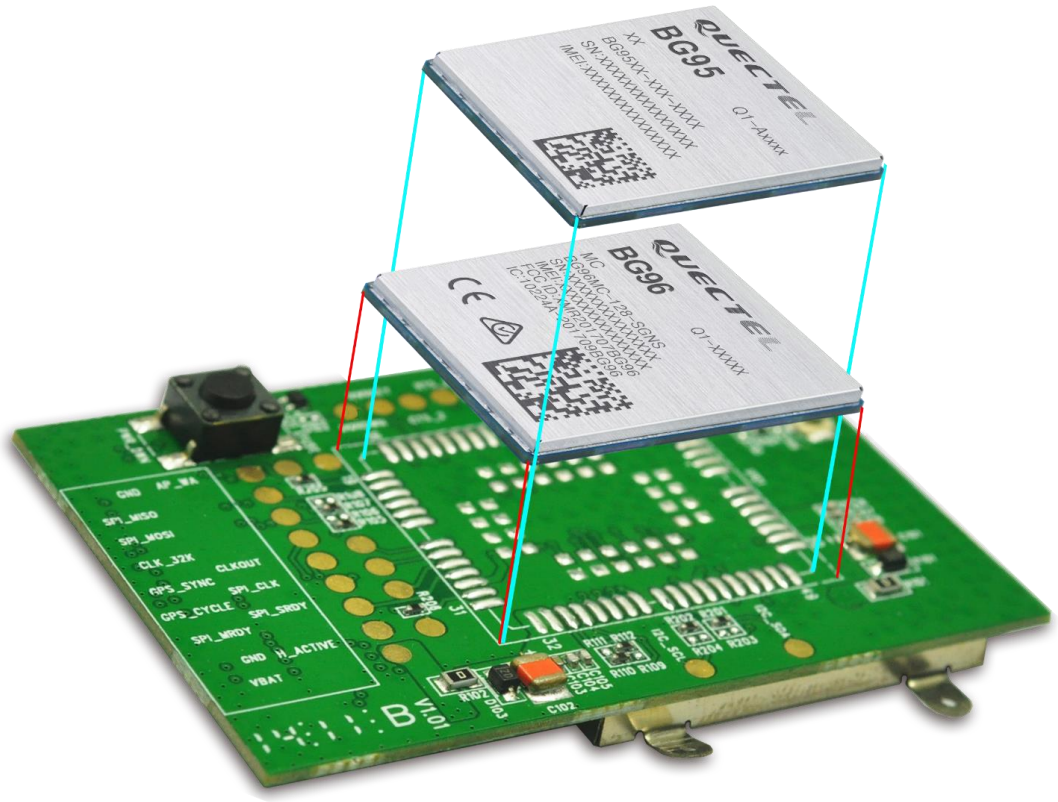


Figure 24: Installation Sketch Map for BG95/BG96

6 Manufacturing and Packaging

6.1. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properly so as to produce a clean stencil surface on a single pass.

It is suggested that the peak reflow temperature is 238ºC~245ºC, and the absolute maximum reflow temperature is 245ºC. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

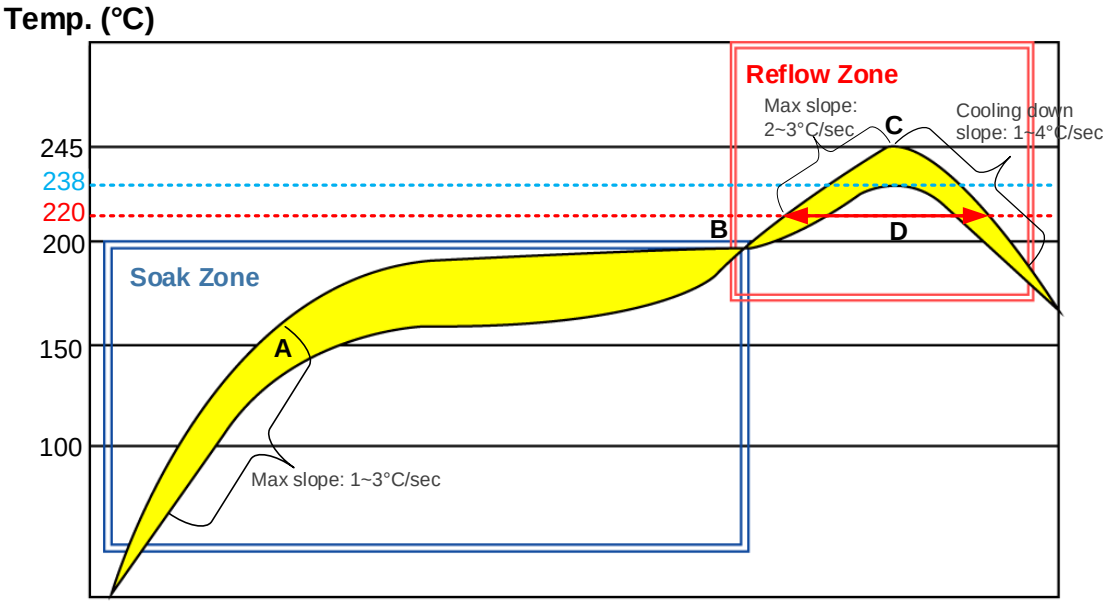


Figure 25: Reflow Soldering Thermal Profile

Table 8: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1 to 3°C/sec
Soak time (between A and B: 150°C and 200°C)	60 to 120 sec
Reflow Zone	
Max slope	2 to 3°C/sec
Reflow time (D: over 220°C)	40 to 60 sec
Max temperature	238°C ~ 245°C
Cooling down slope	1 to 4°C/sec
Reflow Cycle	
Max reflow cycle	1

6.2. Packaging

BG95 and BG96 are packaged in a vacuum-sealed bag which is ESD protected. The bag should not be opened until the devices are ready to be soldered onto the application. The following figures show the packaging details, measured in millimeter (mm).

- **BG96**

The reel is 330mm in diameter and each reel contains 250 modules.

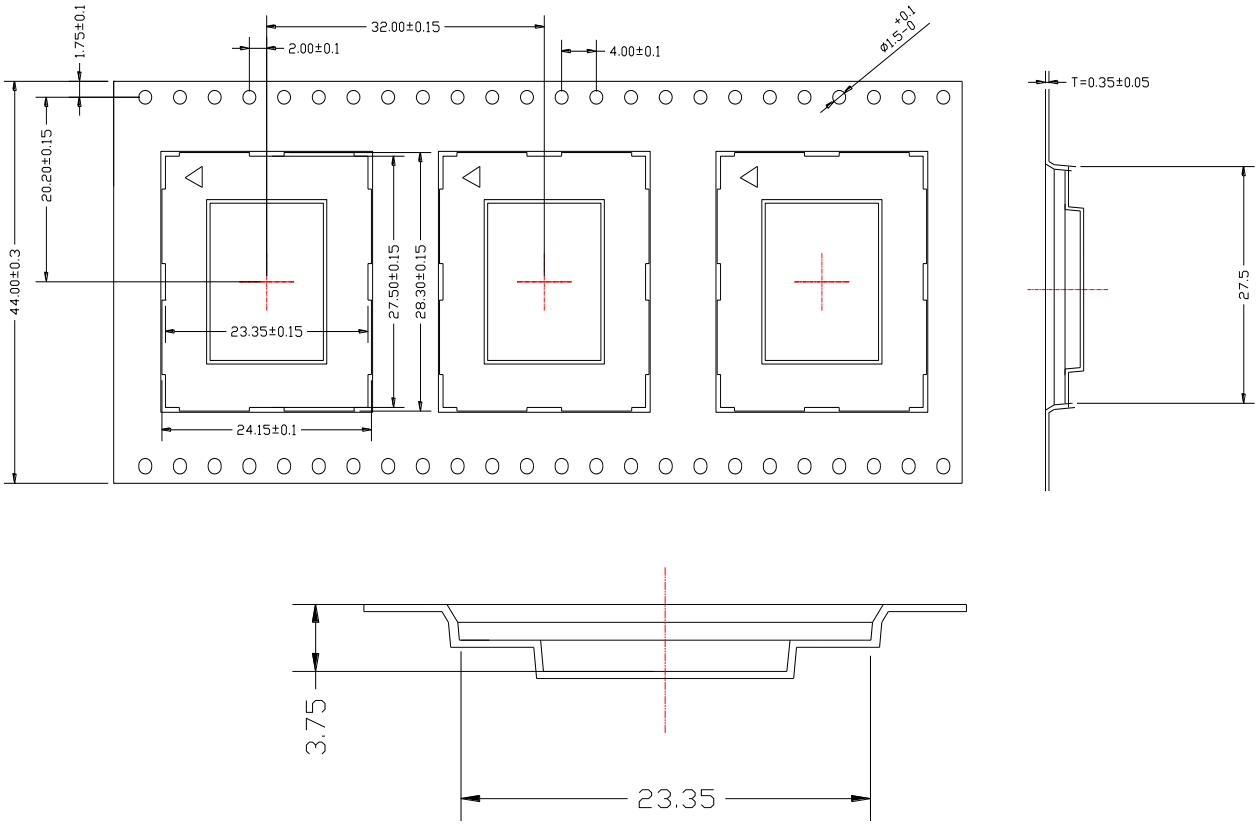


Figure 26: Tape Dimensions of BG96

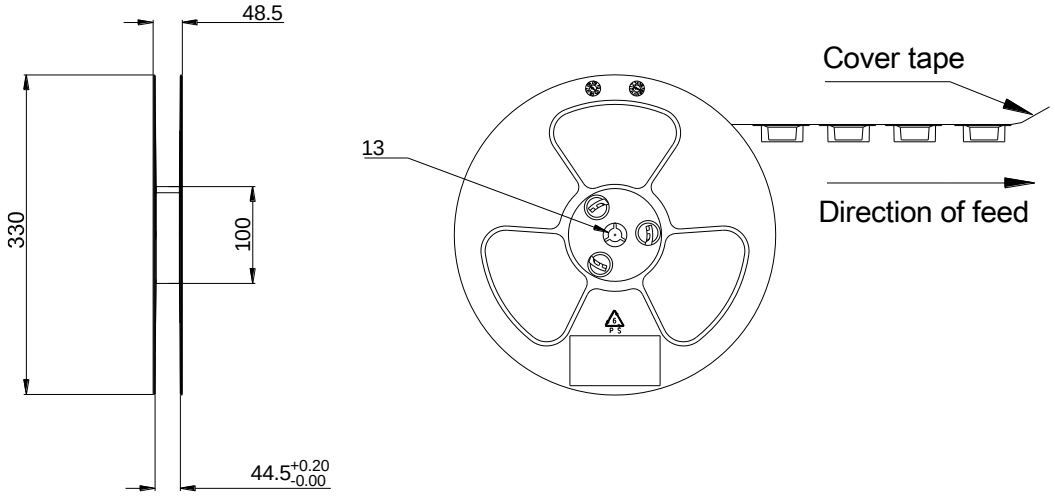


Figure 27: Reel Dimensions of BG96

- **BG95**

The reel is 330mm in diameter and each reel contains 250 modules.

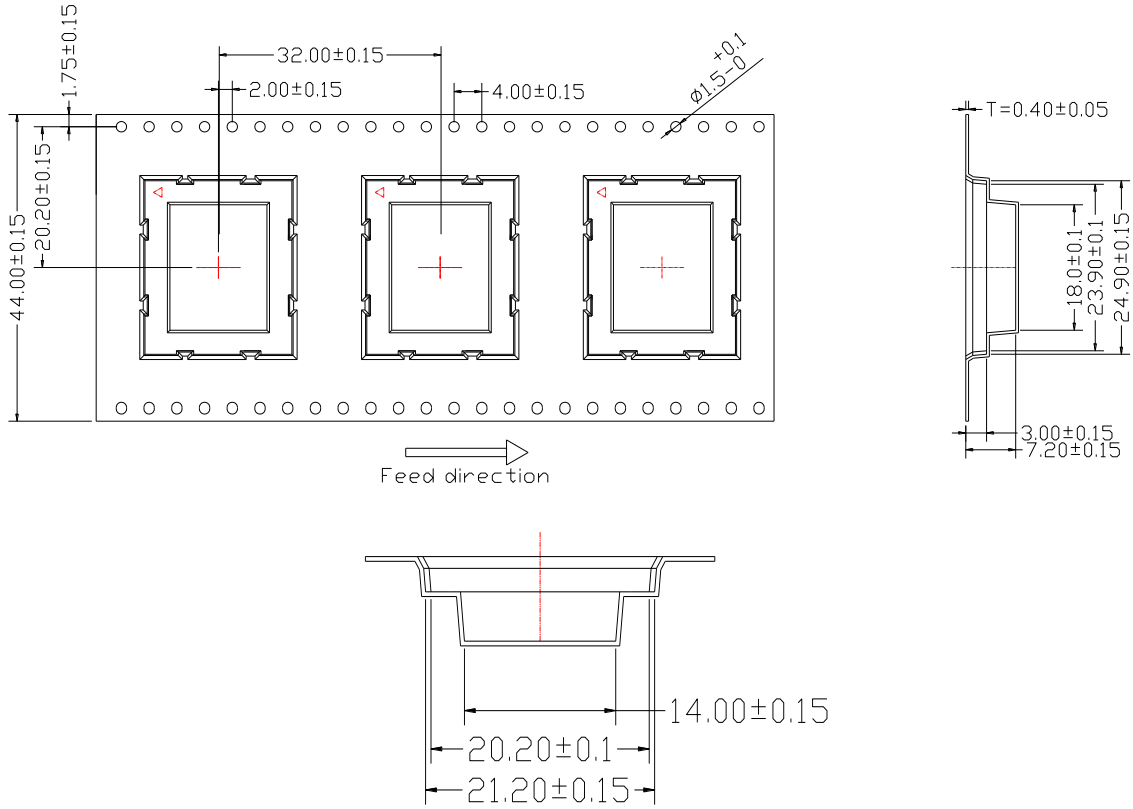


Figure 28: Tape Dimensions of BG95

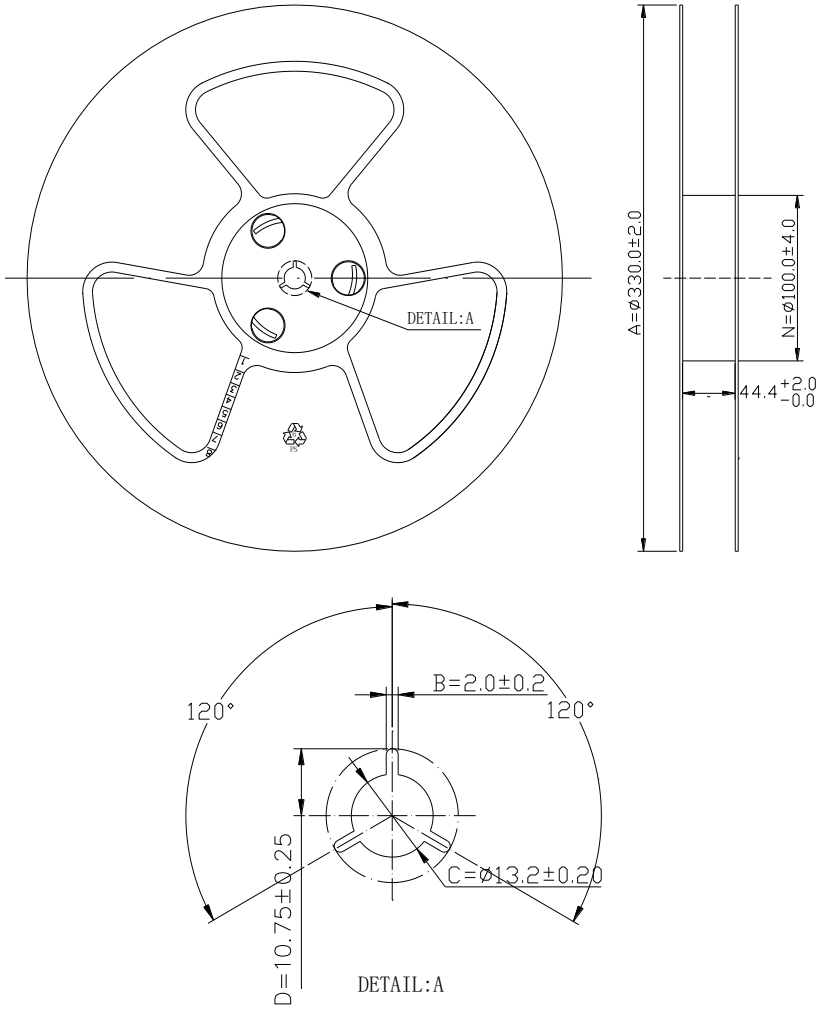


Figure 29: Reel Dimensions of BG95

Table 9: Packaging Specifications of BG95/BG96

Model Name	MOQ for MP	Minimum Package: 250pcs	Minimum Package × 4=1000pcs
BG96	250pcs	Size: 370mm × 350mm × 56mm N.W: 1.0kg G.W: 1.71kg	Size: 380mm × 250mm × 365mm N.W: 4.0kg G.W: 7.16kg
BG95	250pcs	Size: 370mm × 350mm × 56mm N.W: 0.61kg G.W: 1.35kg	Size: 380mm × 250mm × 365mm N.W: 2.45kg G.W: 6.28kg

7 Appendix A References

Table 10: Related Documents

SN	Document Name	Remark
[1]	Quectel_BG96_Hardware_Design	BG96 Hardware Design
[2]	Quectel_BG95_Hardware_Design	BG95 Hardware Design
[3]	Quectel_BG95&BG77_AT_Commands_Manual	BG95/BG77 AT Commands Manual
[4]	Quectel_BG96_AT_Commands_Manual	BG96 AT Commands Manual
[5]	Quectel_Module_Secondary_SMT_User_Guide	Module Secondary SMT User Guide

Table 11: Terms and Abbreviations

Abbreviation	Description
ADC	Analog to Digital Converter
CS	Circuit Switched
CTS	Clear To Send
DFOTA	Delta Firmware upgrade Over-The-Air
DRX	Discontinuous Reception
DTR	Data Terminal Ready
EDGE	Enhanced Data rates for GSM Evolution
EGPRS	Enhanced GPRS
e-I-DRX	Extended Idle Mode Discontinuous Reception
ESD	Electrostatic Discharge
FDD	Frequency Division Duplex

GNSS	Global Navigation Satellite System
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global System for Mobile Communications
HSPA	High Speed Packet Access
I2C	Inter-Integrated Circuit
LDO	Low Dropout Regulator
LED	Light Emitting Diode
LGA	Land Grid Array
LPWA	Low Power Wide Area
LTE	Long Term Evolution
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
QZSS	Quasi-Zenith Satellite System
RF	Radio Frequency
RTS	Request To Send
SMS	Short Message Service
TDD	Time Division Duplexing
UART	Universal Asynchronous Receiver/Transmitter
UMTS	Universal Mobile Telecommunications System
USB	Universal Serial Bus
(U)SIM	(Universal) Subscriber Identity Module